

Revision : 1.01

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09	DDRIII CHANNEL B
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25	AUDIO JACK

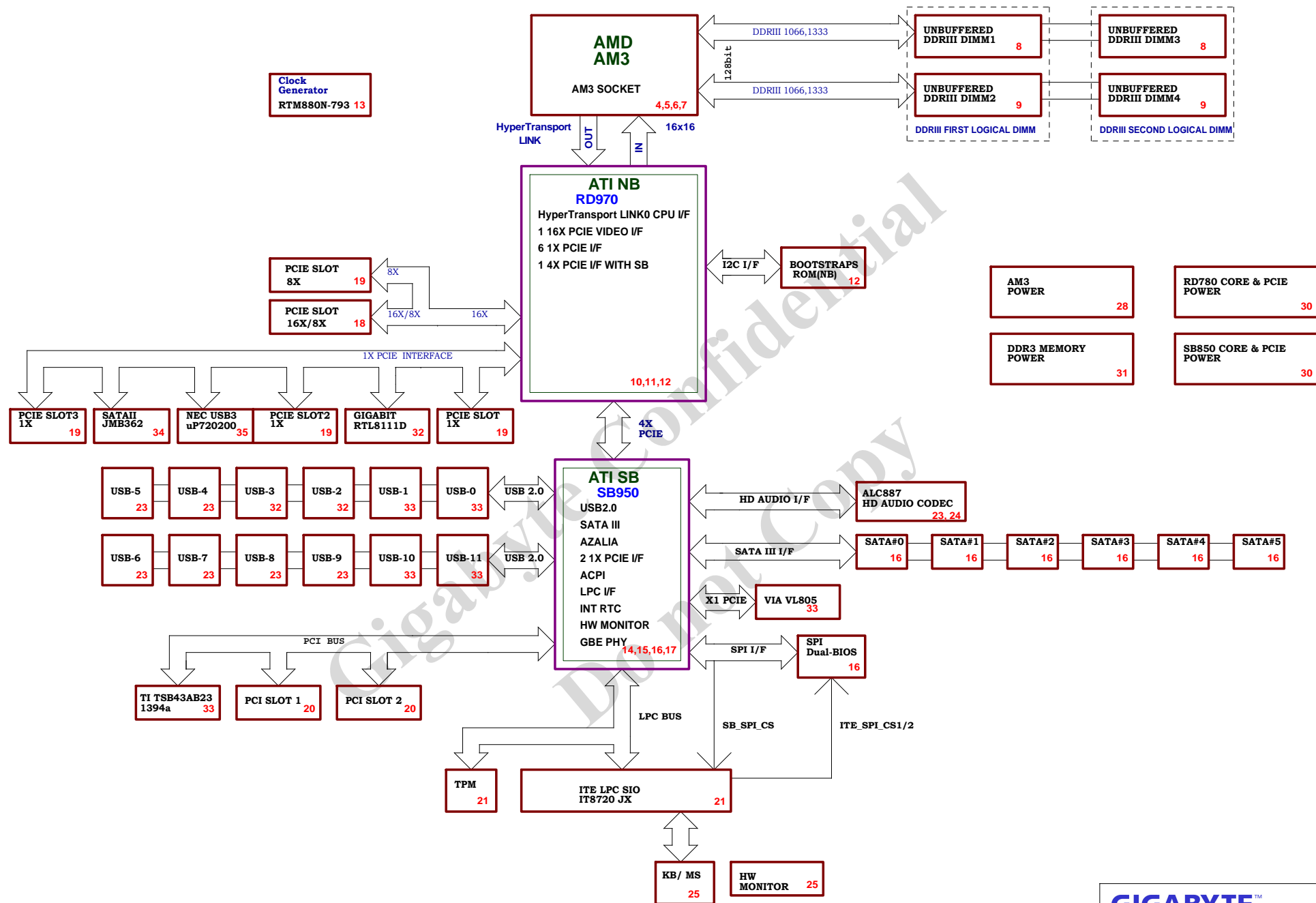
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P-Code: U98094-0

[illegible]

Circuit or PCB layout change for next version

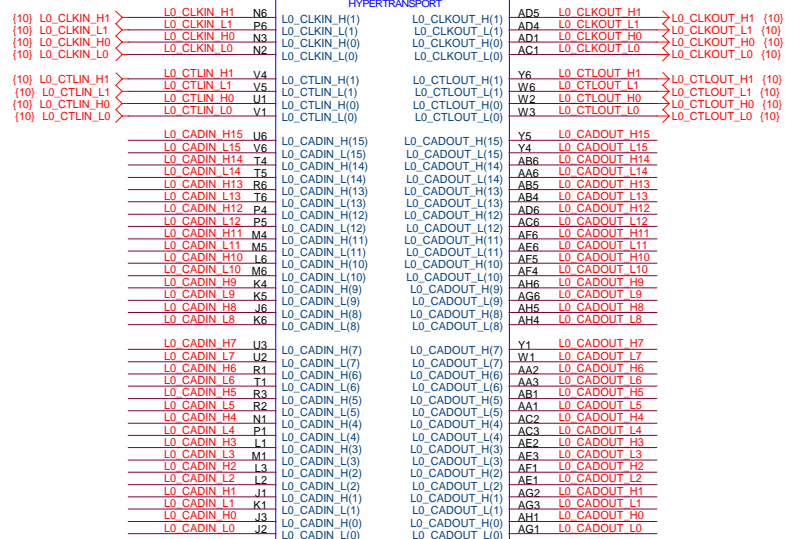
[illegible]



L0_CADIN_L[0..15] < L0_CADIN_L[0..15] (10)
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] (10)
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] (10)
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] (10)

M2CPUA

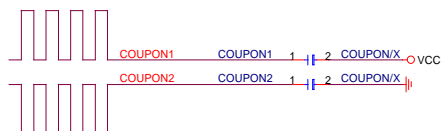
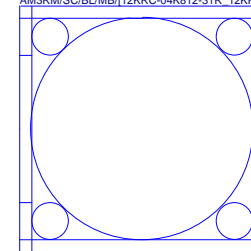
HYPERTRANSPORT



CPU-SK/942AM3b/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

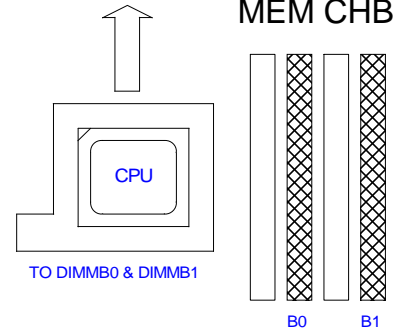
CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

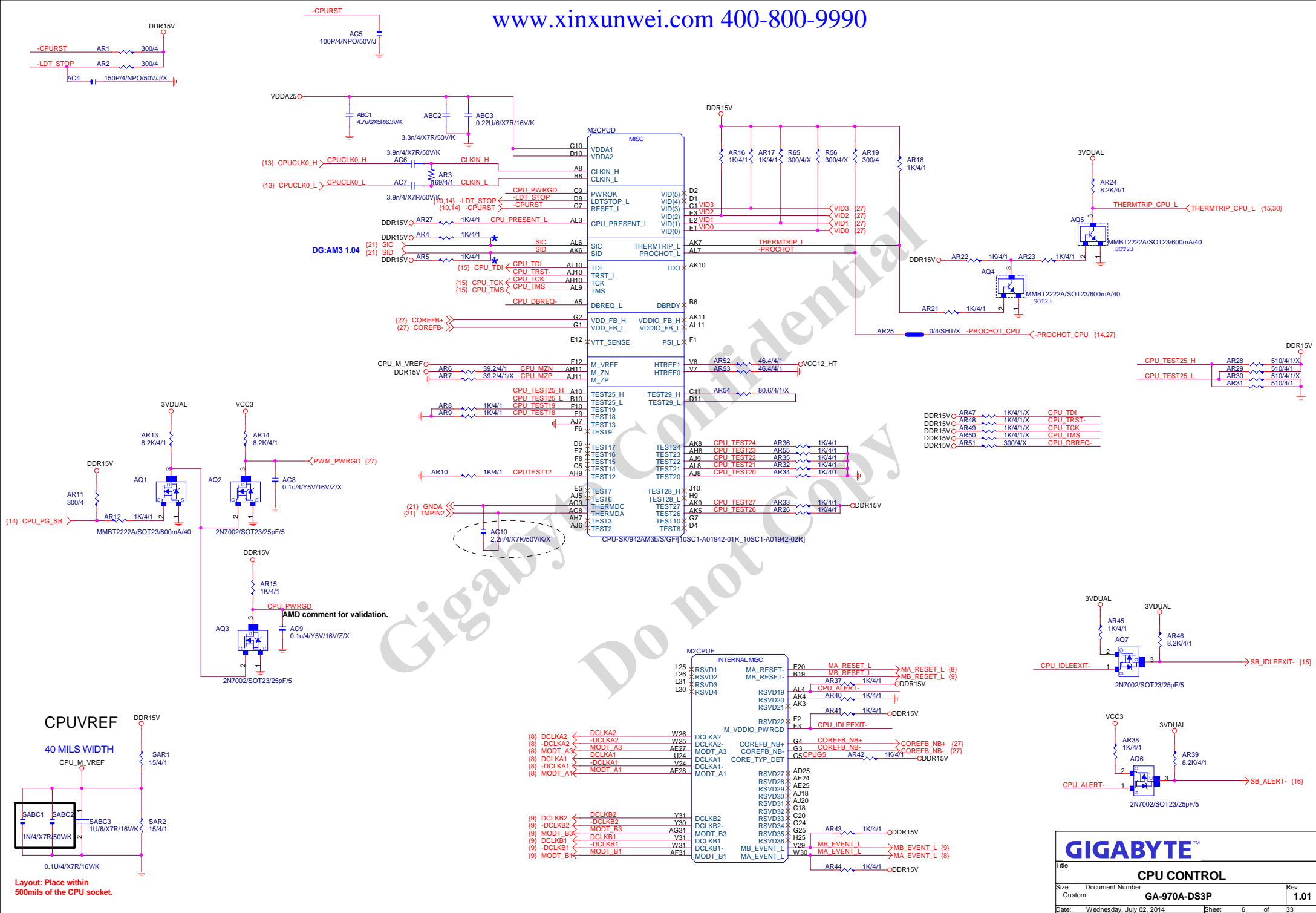
VLDT_A = VCC12_HT
 VLDT_B = HT12B

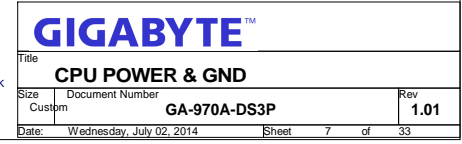
M2CPU
AM3RM/SC/BL/MB/[12KRC-04K812-31R_12KRC-04K812-32R]

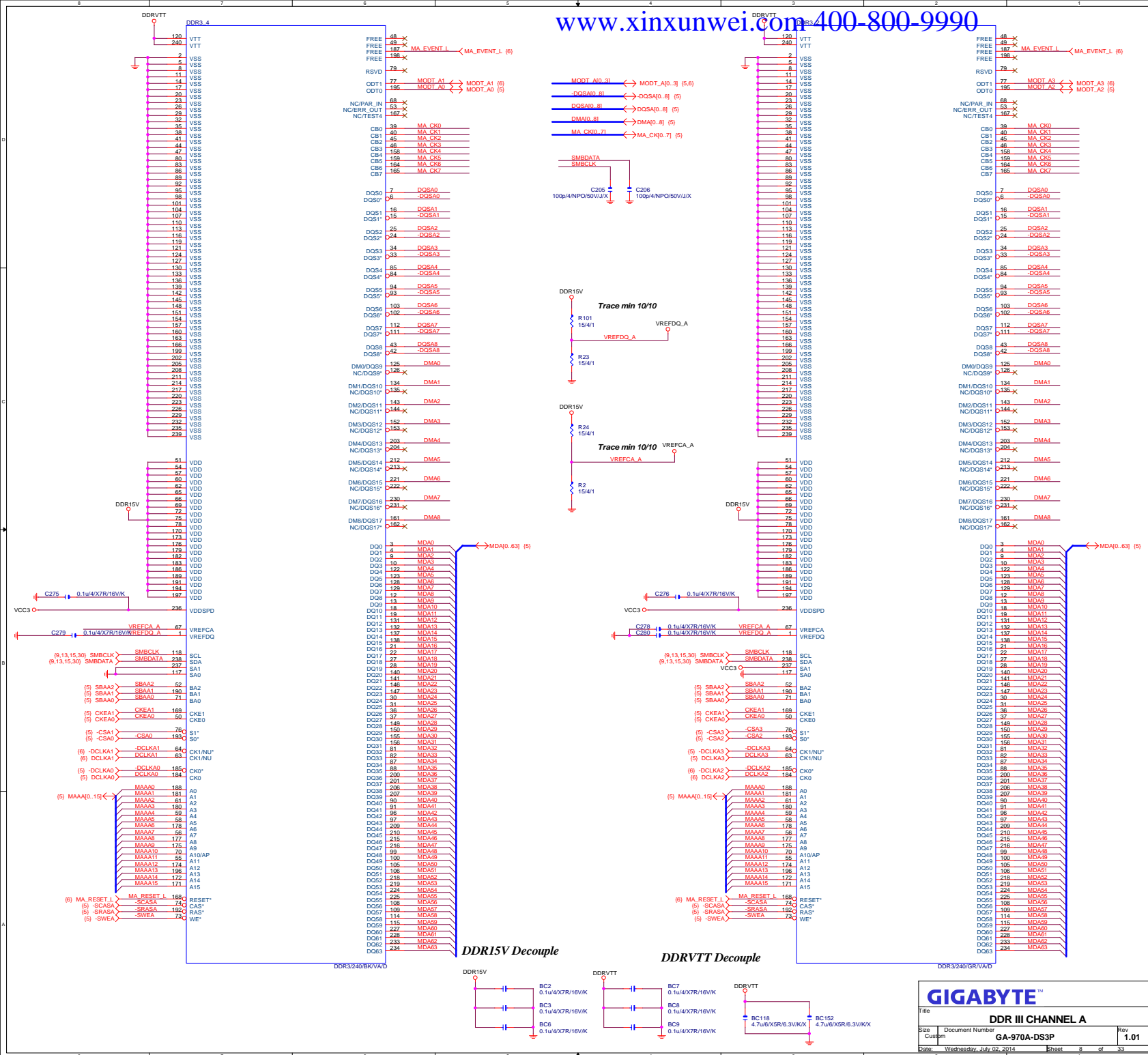
GIGABYTE™

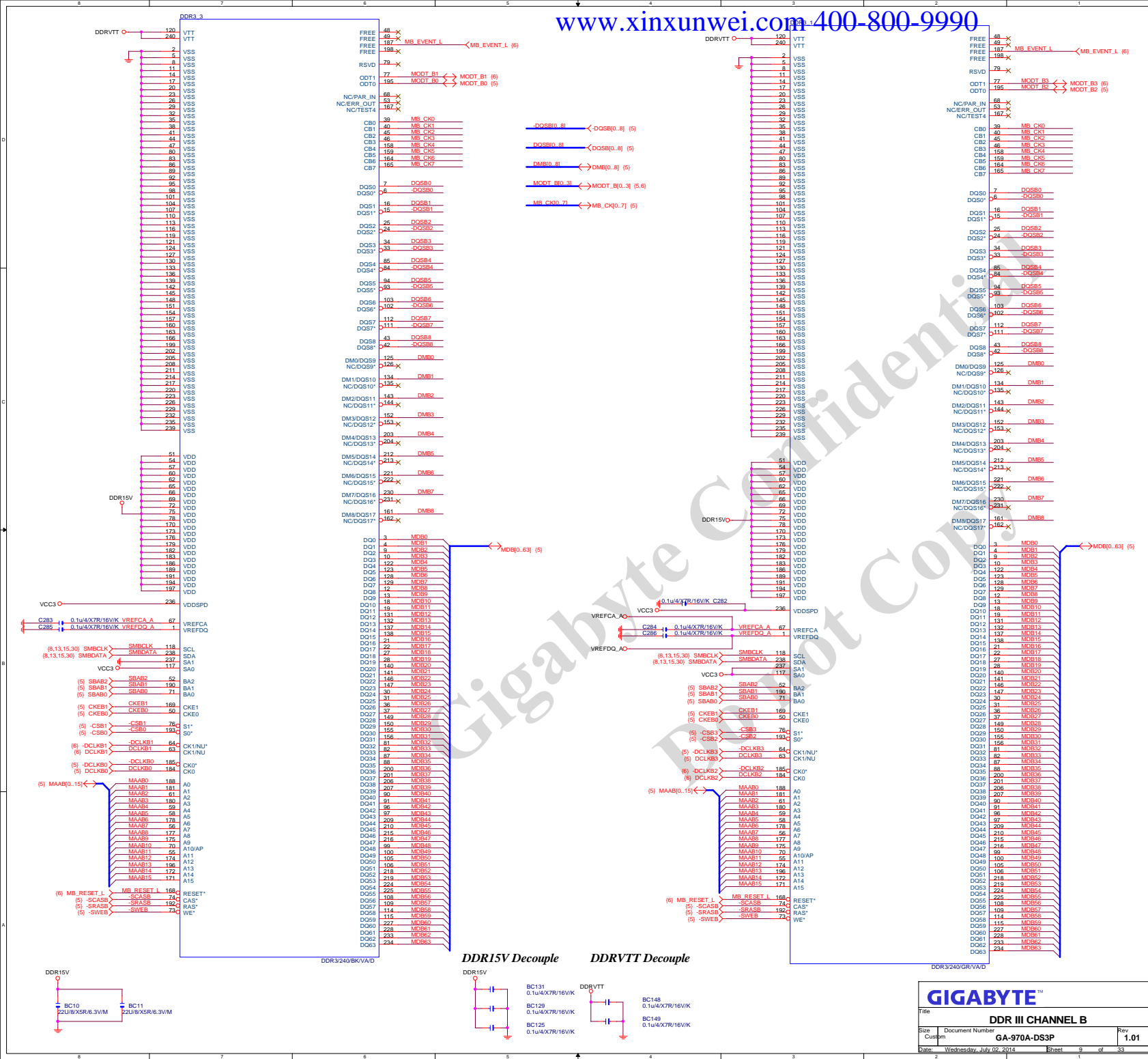
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CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custpm	GA-970A-DS3P	1.01	
Date:	Wednesday, July 02, 2014	Sheet	4 of 33

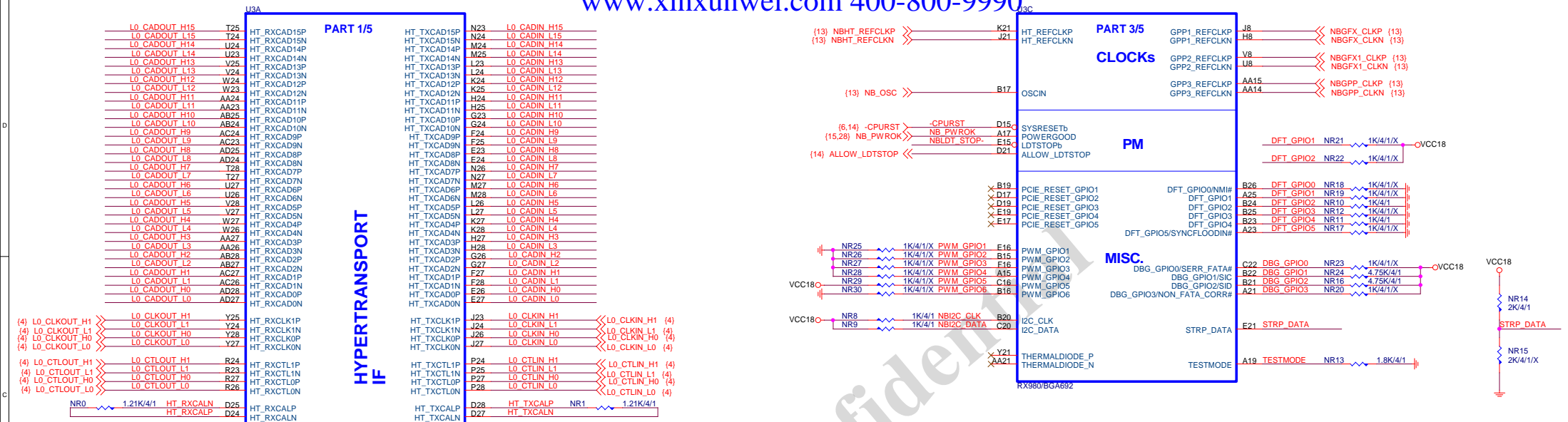














U3B

PART 2/5

EXP A_RXP15 N6
EXP A_RXN15 N5
EXP A_RXP14 M5
EXP A_RXN14 M4
EXP A_RXP13 L6
EXP A_RXN13 L5
EXP A_RXP12 K5
EXP A_RXN12 K4
EXP A_RXP11 J6
EXP A_RXN11 J5
EXP A_RXP10 H5
EXP A_RXN10 H4
EXP A_RXP9 G6
EXP A_RXN9 G5
EXP A_RXP8 F5
EXP A_RXN8 F4
EXP A_RXP7 D2
EXP A_RXN7 D1
EXP A_RXP6 B5
EXP A_RXN6 B4
EXP A_RXP5 C6
EXP A_RXN5 E6
EXP A_RXP4 E7
EXP A_RXN4 F7
EXP A_RXP3 D8
EXP A_RXN3 E8
EXP A_RXP2 E9
EXP A_RXN2 F9
EXP A_RXP1 D10
EXP A_RXN1 E10
EXP A_RXP0 E11
EXP A_RXN0 F11

AC9
AD9
AE8
AC7
AD7
AD6
AE6
AE5
AG5
AF2
AD2
AD1
AB5
AB4
AA6
AA5
Y5
Y4
W6
W5
V5
V4
U6
U5
T5
T4
R6
R5
P5
P4

AD11
AC11
AE12
AD12
AD13
AC13
AE14
AD14
AD15
AC15
AE16
AD16
AD17
AC17
AE18
AD18
AD19
AC19
AH20
AG20

AC21
AD21
AE22
AF25
AG25
AG26
AH26

AE20
AD20
AE10
AD10
F14
E14

RX980/BGA692

PCIE
GPP1PCIE
GPP2PCIE
GPP3PCIE
ALINK

GPP1_RX15P
GPP1_RX15N
GPP1_RX14P
GPP1_RX14N
GPP1_RX13P
GPP1_RX13N
GPP1_RX12P
GPP1_RX12N
GPP1_RX11P
GPP1_RX11N
GPP1_RX10P
GPP1_RX10N
GPP1_RX9P
GPP1_RX9N
GPP1_RX8P
GPP1_RX8N
GPP1_RX7P
GPP1_RX7N
GPP1_RX6P
GPP1_RX6N
GPP1_RX5P
GPP1_RX5N
GPP1_RX4P
GPP1_RX4N
GPP1_RX3P
GPP1_RX3N
GPP1_RX2P
GPP1_RX2N
GPP1_RX1P
GPP1_RX1N
GPP1_RX0P
GPP1_RX0N

GPP2_RX15P
GPP2_RX15N
GPP2_RX14P
GPP2_RX14N
GPP2_RX13P
GPP2_RX13N
GPP2_RX12P
GPP2_RX12N
GPP2_RX11P
GPP2_RX11N
GPP2_RX10P
GPP2_RX10N
GPP2_TX9P
GPP2_TX9N
GPP2_TX8P
GPP2_TX8N
GPP2_TX7P
GPP2_TX7N
GPP2_TX6P
GPP2_TX6N
GPP2_TX5P
GPP2_TX5N
GPP2_TX4P
GPP2_TX4N
GPP2_TX3P
GPP2_TX3N
GPP2_TX2P
GPP2_TX2N
GPP2_TX1P
GPP2_TX1N
GPP2_TX0P
GPP2_TX0N

GPP3_RX9P
GPP3_RX9N
GPP3_RX8P
GPP3_RX8N
GPP3_RX7P
GPP3_RX7N
GPP3_RX6P
GPP3_RX6N
GPP3_RX5P
GPP3_RX5N
GPP3_RX4P
GPP3_RX4N
GPP3_RX3P
GPP3_RX3N
GPP3_RX2P
GPP3_RX2N
GPP3_RX1P
GPP3_RX1N
GPP3_RX0P
GPP3_RX0N

SB_RX3P
SB_RX3N
SB_RX2P
SB_RX2N
SB_RX1P
SB_RX1N
SB_RX0P
SB_RX0N

PCE_BCALRP
PCE_BCALRN
PCE_RCALRP
PCE_RCALRN
PCE_TCALRP
PCE_TCALRN

RX980/BGA692

N3
M2
M1
L3
L2
K2
K1
J3
J2
H2
H1
G3
G2
F2
F1
E3
E2
A4
B4
A6
B6
B7
C7
A8
B8
C9
B9
C9
A10
B10
B11
C11

AF9
AG9
AG8
AH8
AF7
AG7
AG6
AH6
AG4
AH4
AE3
AE2
AC3
AC2
AB2
AB1
AA3
AA2
Y2
Y1
W3
W2
V2
V1
U3
U2
T2
T1
R3
R2
P2
P1

AH10
AG10
AG11
AE15
AH12
AG12
AG13
AE13
AH14
AG14
AG15
AF15
AH15
AG16
AG17
AH17
AG18
AG19
AF19

AG22
AH22
AF21
AG21
AF23
AG23
AG24
AH24

NC11
NC12
NC14
NC13
NC15
NC16
NC18
NC17

RX980/BGA692

PCI_E slot TX need CAP close to slot side

GPP TX5P C NC4 0.1u/4/X7R/16V/K PCIE5_OP (19)
GPP TX5N C NC3 0.1u/4/X7R/16V/K PCIE5_ON (19)
GPP TX4P C NC6 0.1u/4/X7R/16V/K ML_OP (32)
GPP TX4N C NC5 0.1u/4/X7R/16V/K ML_ON (32)
GPP TX2P C NC10 0.1u/4/X7R/16V/K PCIE2_OP (19)
GPP TX2N C NC9 0.1u/4/X7R/16V/K PCIE2_ON (19)
GPP TX1P C NC20 0.1u/4/X7R/16V/K PCIE1_OP (19)
GPP TX1N C NC19 0.1u/4/X7R/16V/K PCIE1_ON (19)
GPP TX0P C NC2 0.1u/4/X7R/16V/K USB3_OP (33)
GPP TX0N C NC1 0.1u/4/X7R/16V/K USB3_ON (33)

A TX3P C NC11 0.1u/4/X7R/16V/K A_TX3P (14)
A_TX3N C NC12 0.1u/4/X7R/16V/K A_TX3N (14)
A_TX2P C NC14 0.1u/4/X7R/16V/K A_TX2P (14)
A_TX2N C NC13 0.1u/4/X7R/16V/K A_TX2N (14)
A_TX1P C NC15 0.1u/4/X7R/16V/K A_TX1P (14)
A_TX1N C NC16 0.1u/4/X7R/16V/K A_TX1N (14)
A_TX0P C NC18 0.1u/4/X7R/16V/K A_TX0P (14)
A_TX0N C NC17 0.1u/4/X7R/16V/K A_TX0N (14)

PLACE THESE CAP CLOSE TO NB.

EXP A_TXP0..15] >> EXP_A_TXP[0..15] (18)

EXP A_TXN0..15] >> EXP_A_TXN[0..15] (18)

EXP A_RXP0..15] >> EXP_A_RXP[0..15] (18)

EXP A_RXN0..15] >> EXP_A_RXN[0..15] (18)

NB_VCC O
NR2 1.27K/4/1 AE20
NR3 1.82K/4/1 AD20
NR4 1.27K/4/1 AE10
NR5 1.82K/4/1 AD10
NR6 1.27K/4/1 F14
NR7 1.82K/4/1 E14

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Title RS780 PCIE I/F ,Switch

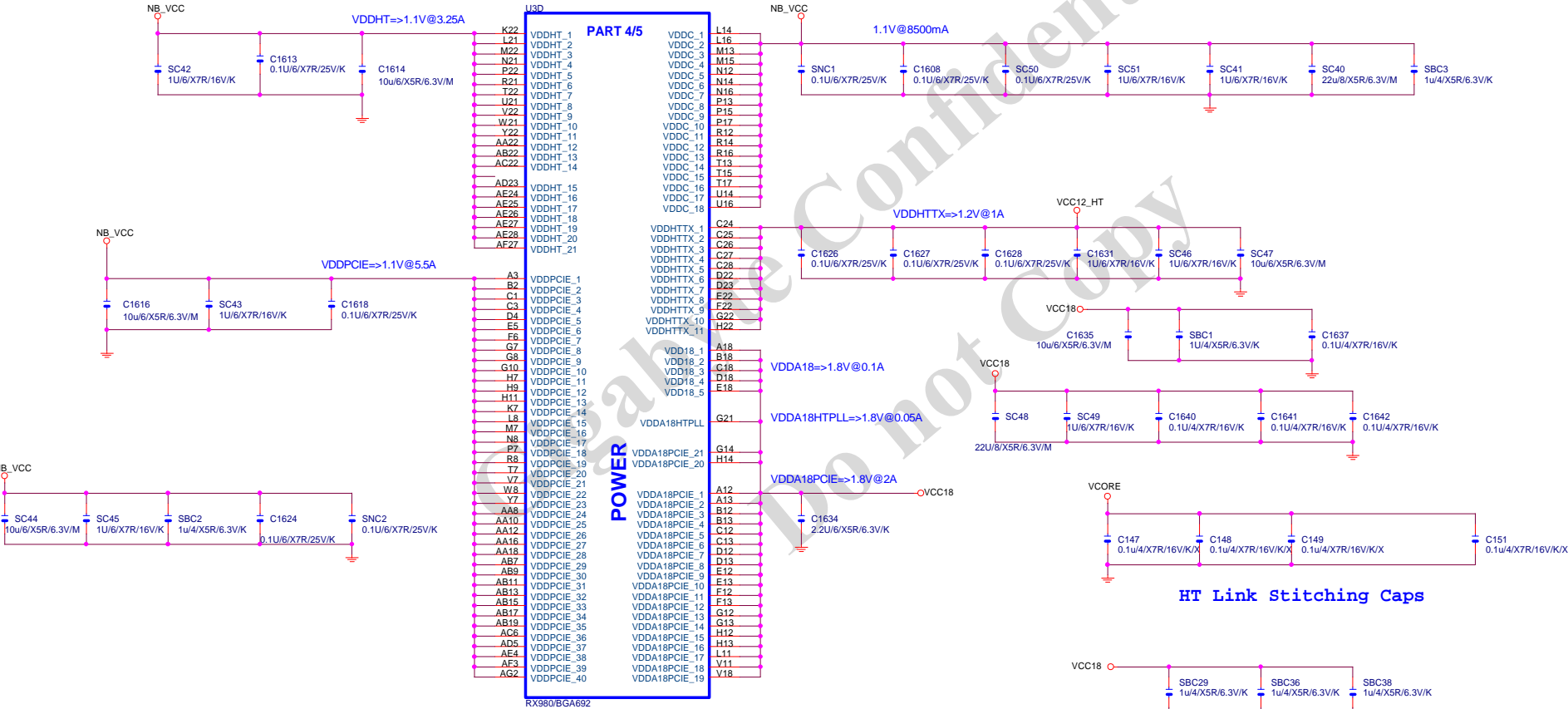
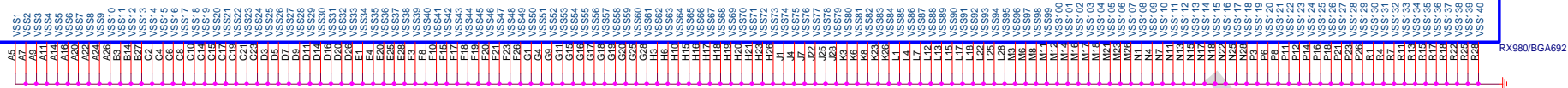
Size Document Number GA-970A-DS3P

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PART 5/5

GROUND



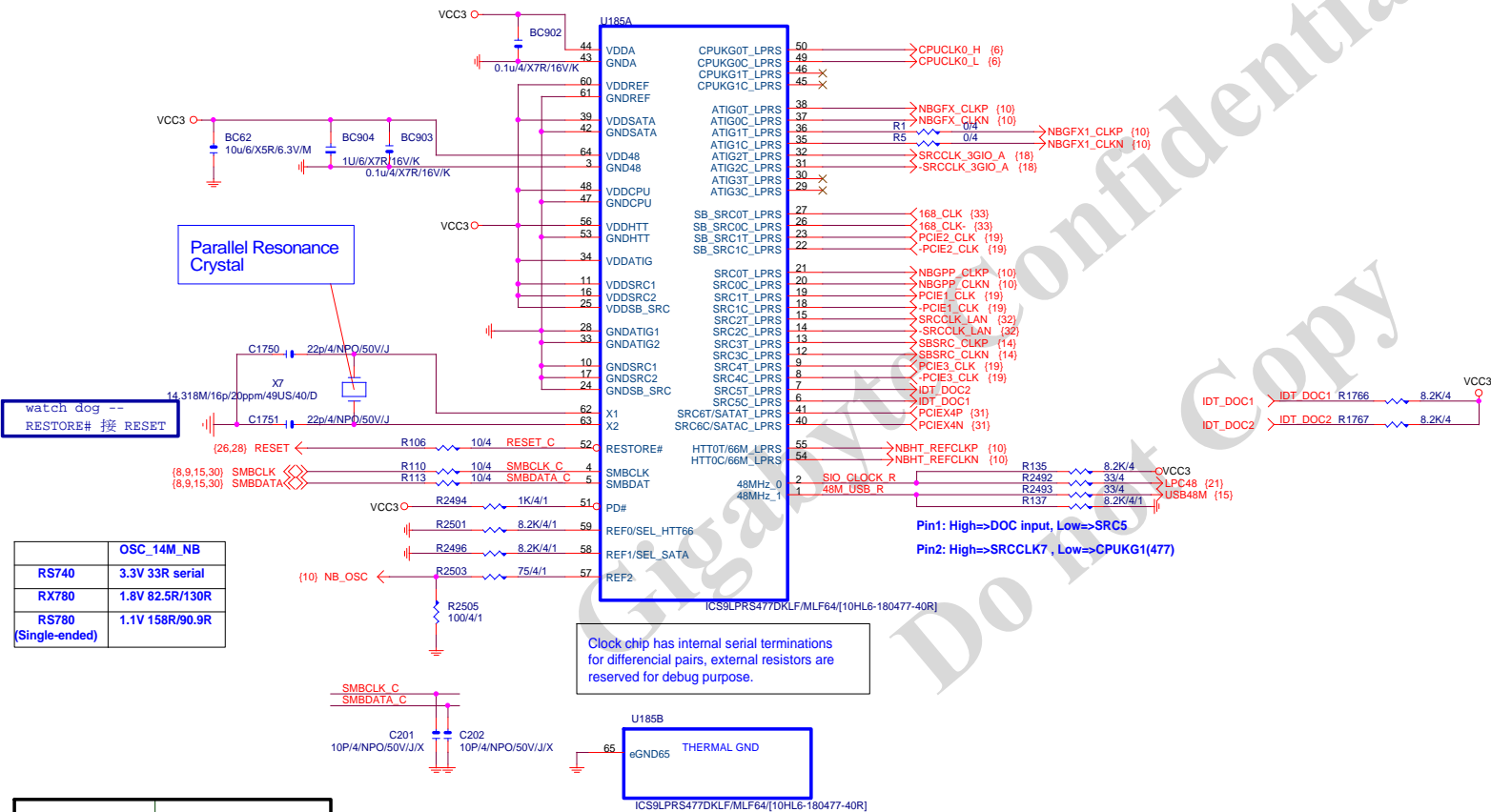
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
 R851 less than 100 mils away from R800/801
 route CPU clock as 100ohm differential pair

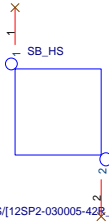


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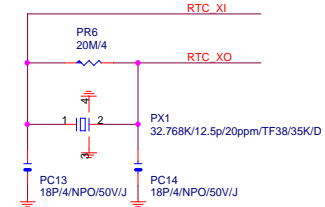
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Size	Document Number	GA-970A-DS3P			Rev
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PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

S.B HEATSINK



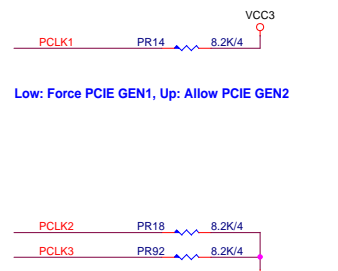
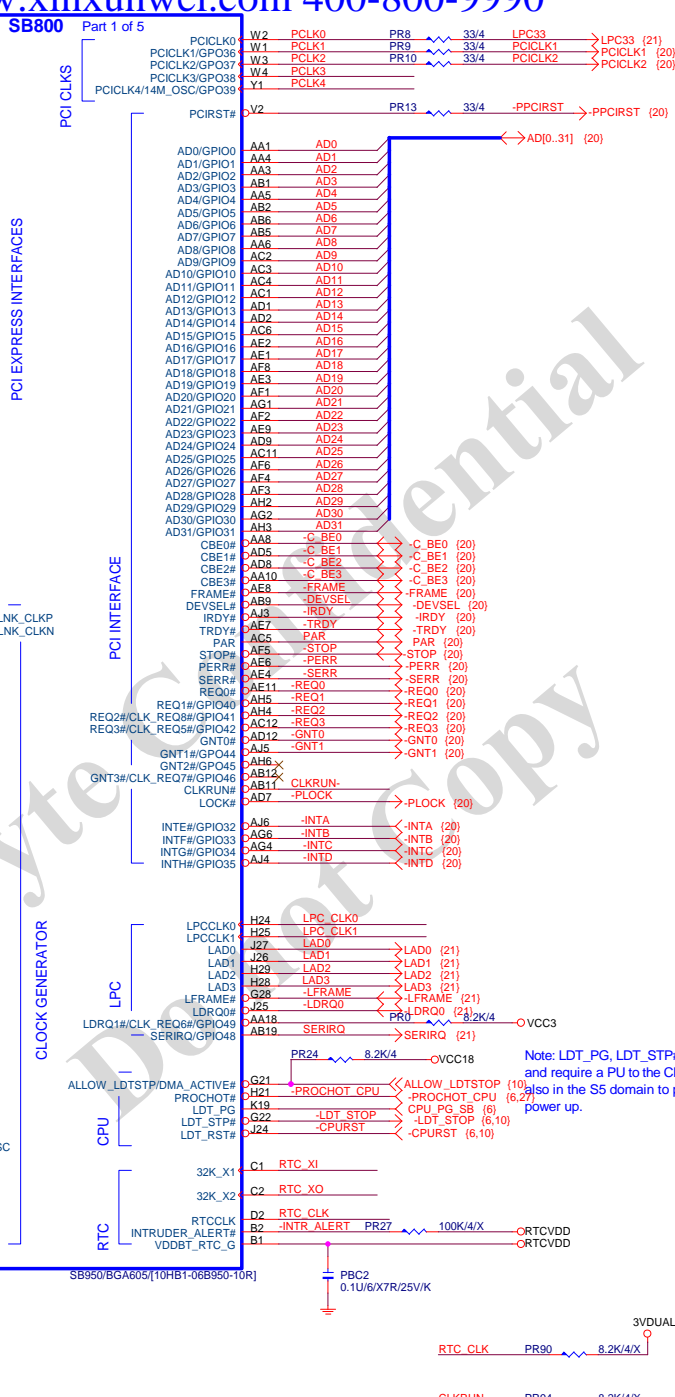
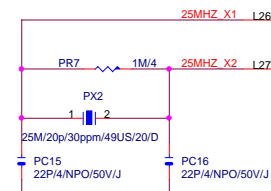
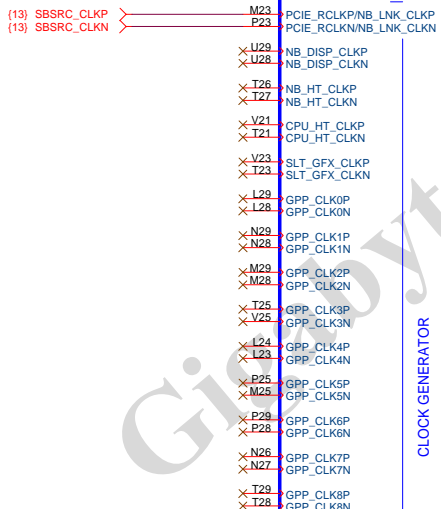
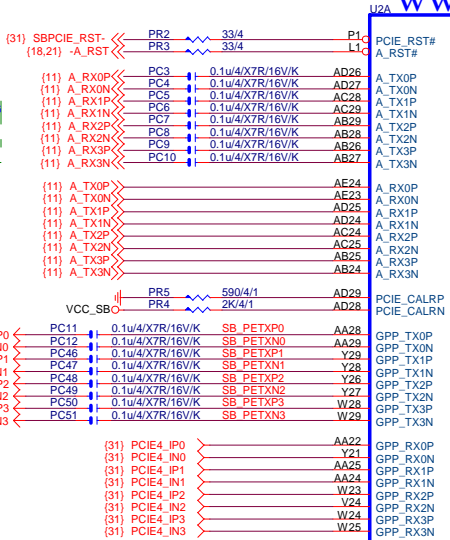
SB_HS/[12SP2-030005-42R_12SP2-030005-43R]



PX1



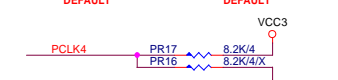
SHW/D0.64*5.08*6.74



Low: Force PCIE GEN1, Up: Allow PCIE GEN2



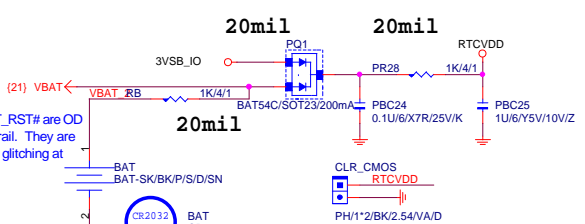
	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT



BIOS after boot setting
EC AOD-ACC



	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED	CLKGEN DISABLED
	DEFAULT	DEFAULT



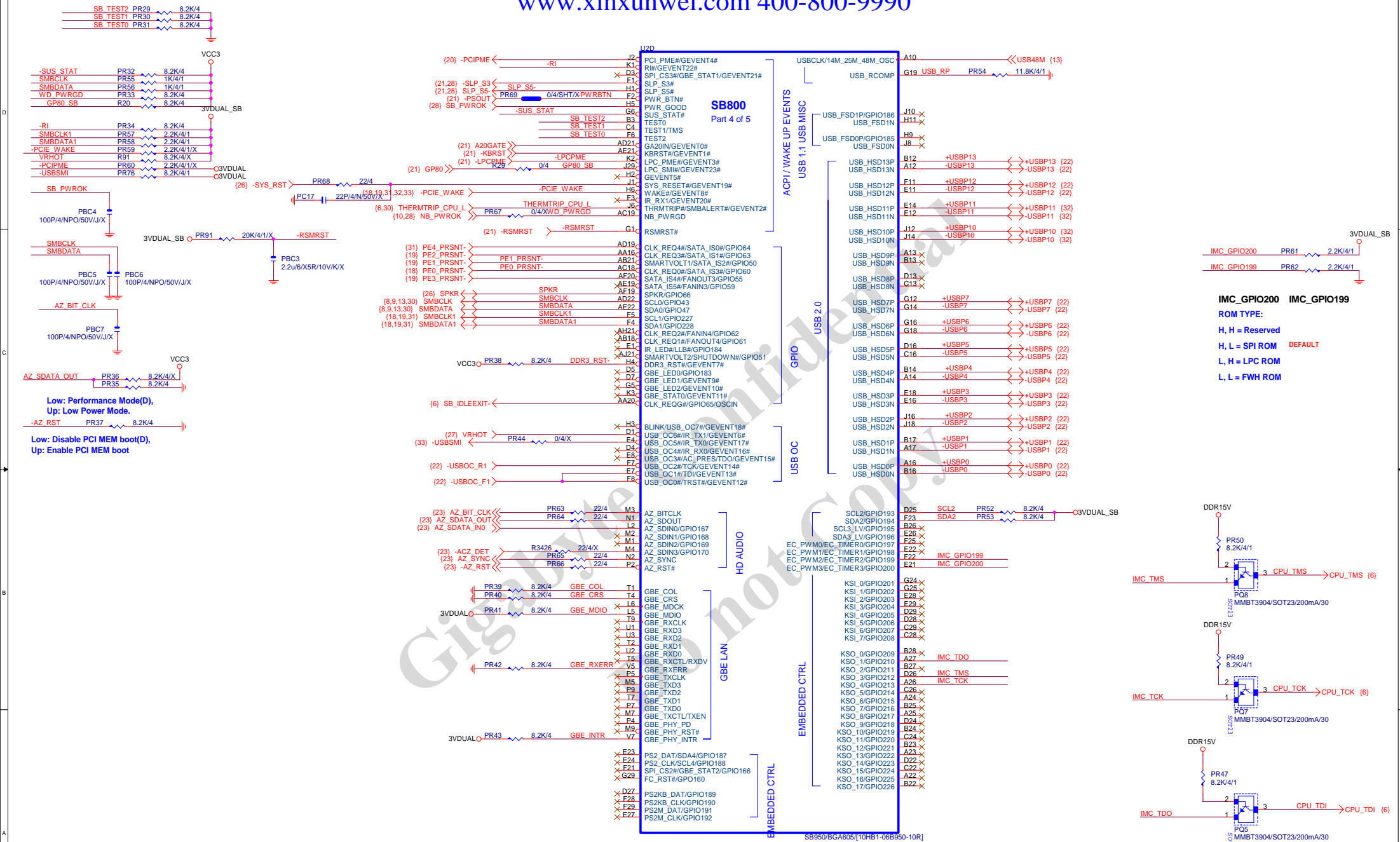
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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ATI SB700 PCIE/PCI/CPU/LPC

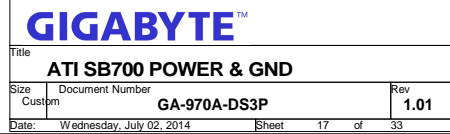
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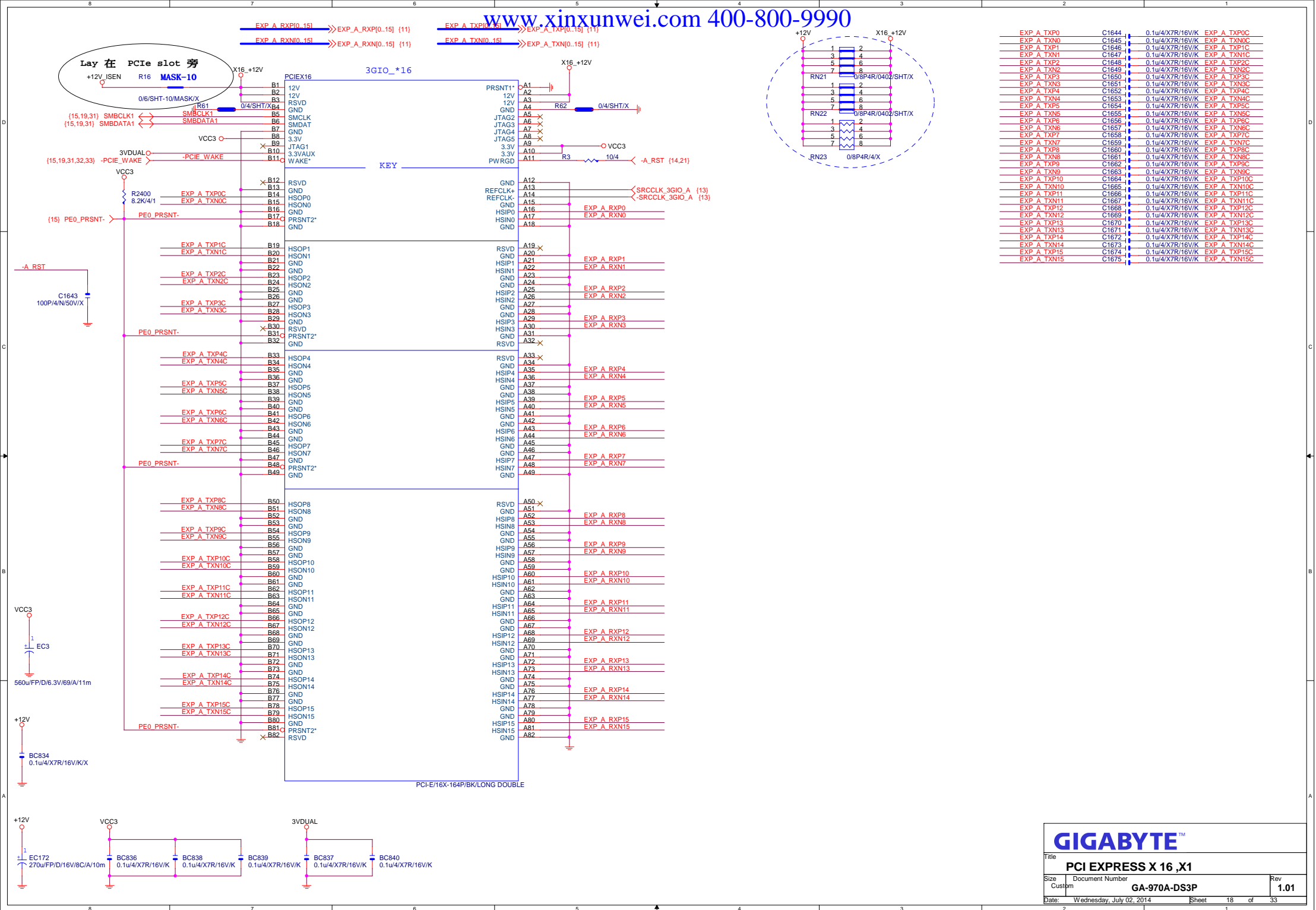


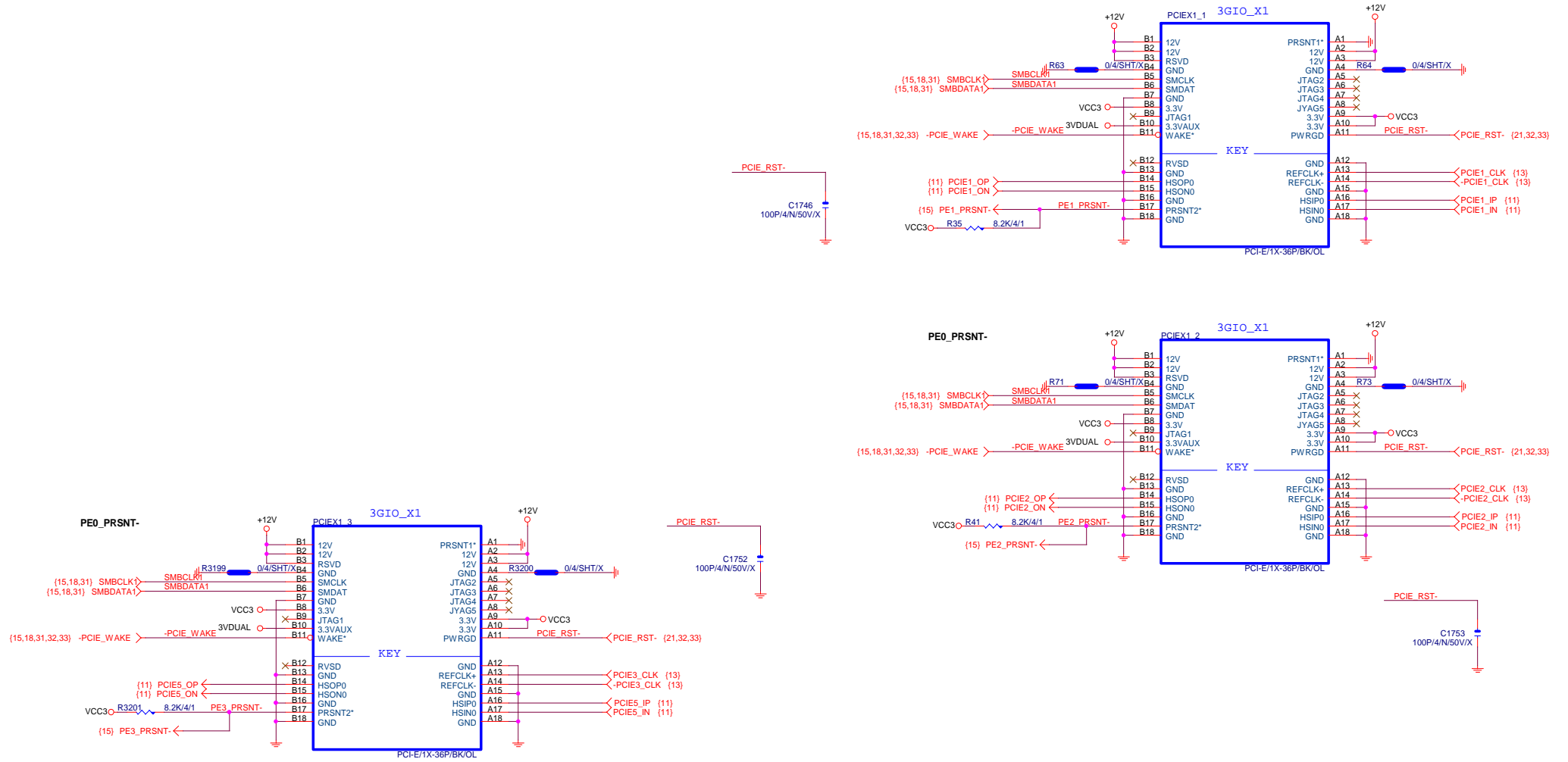
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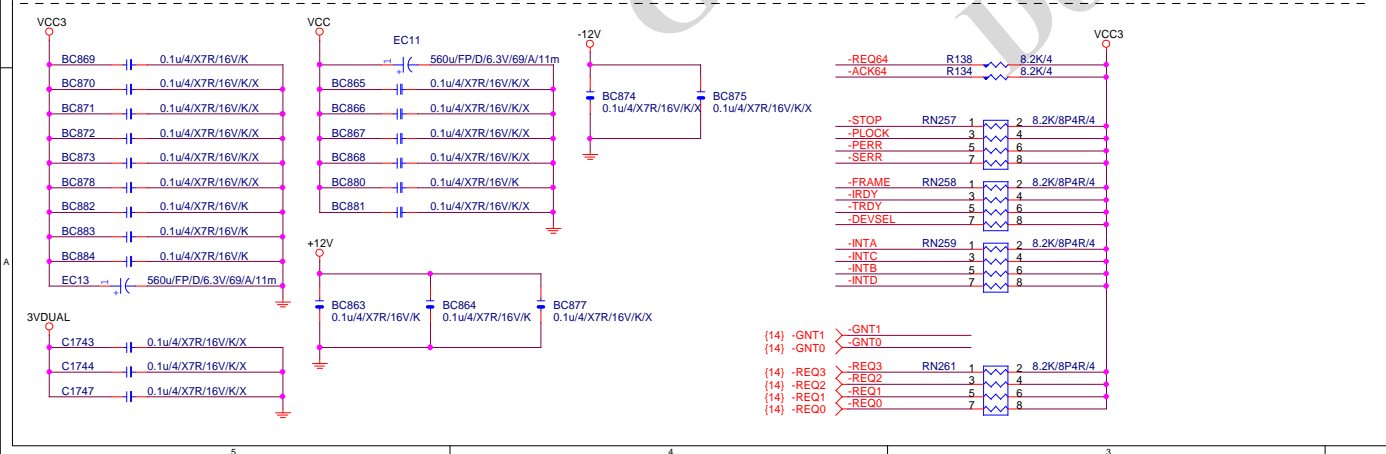
ATI SB700 ACPI/USB/GPIO/AUDIO

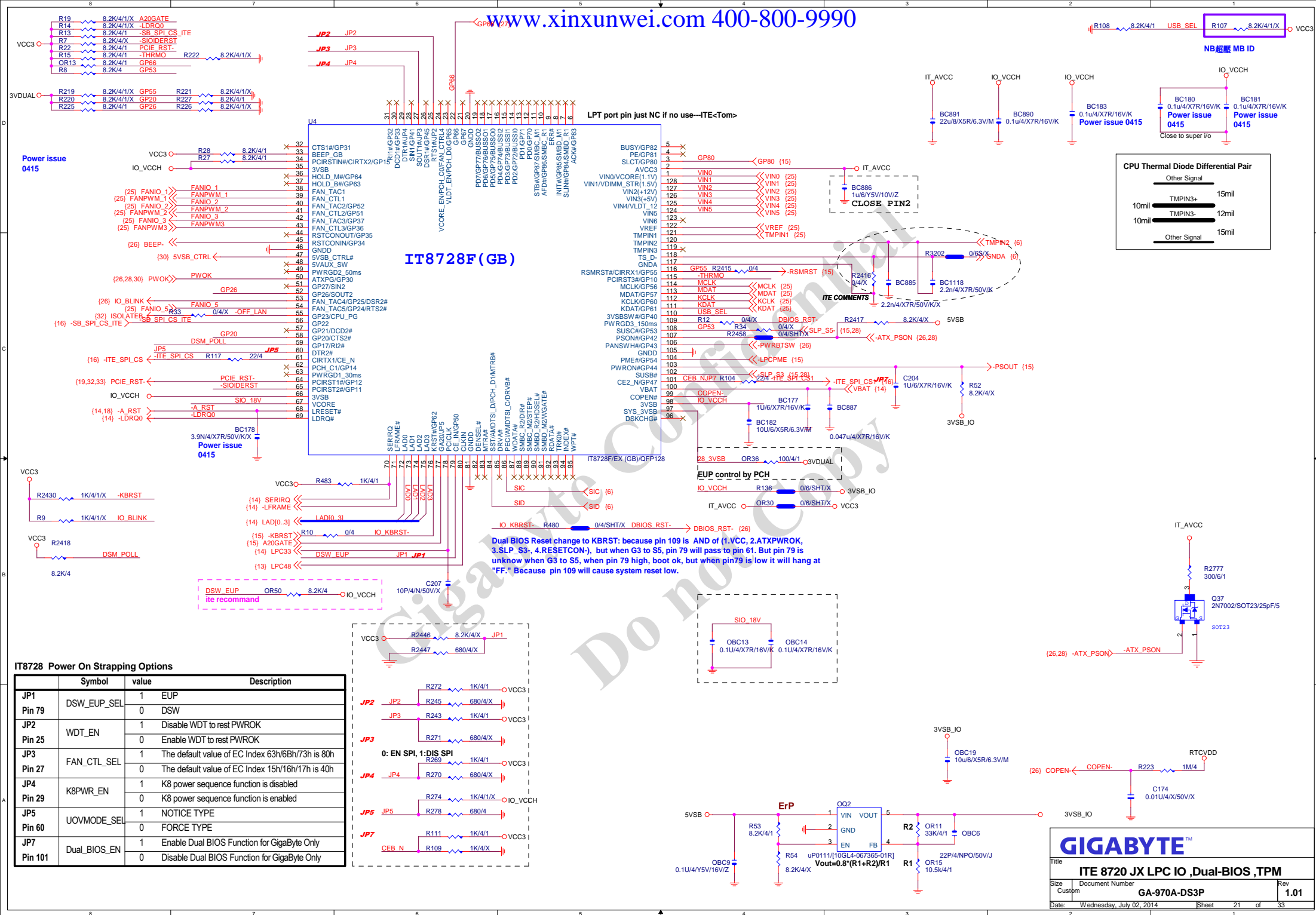
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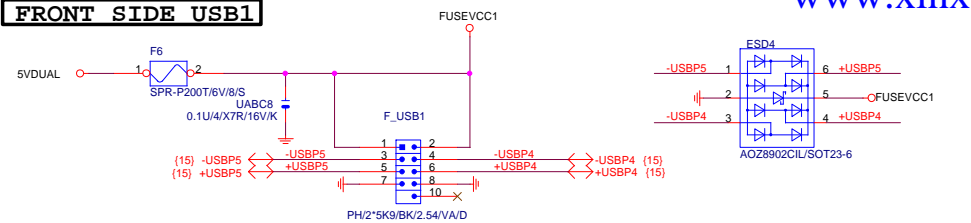




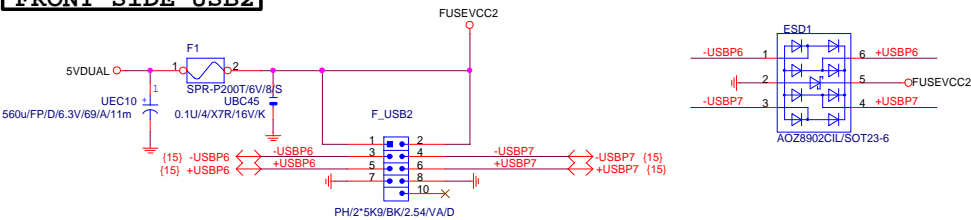




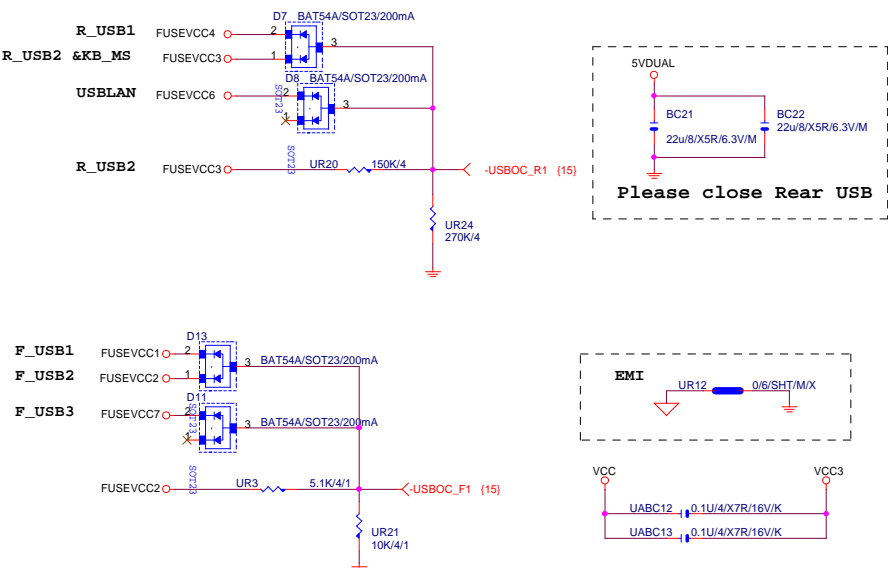
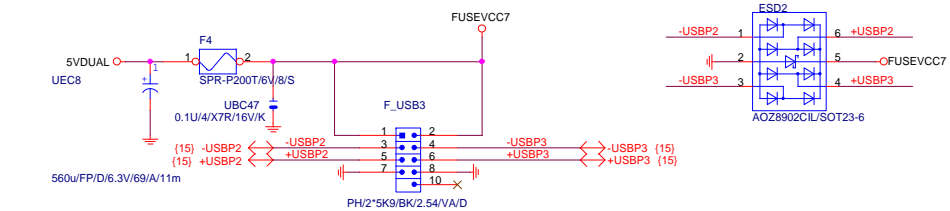
FRONT SIDE USB1



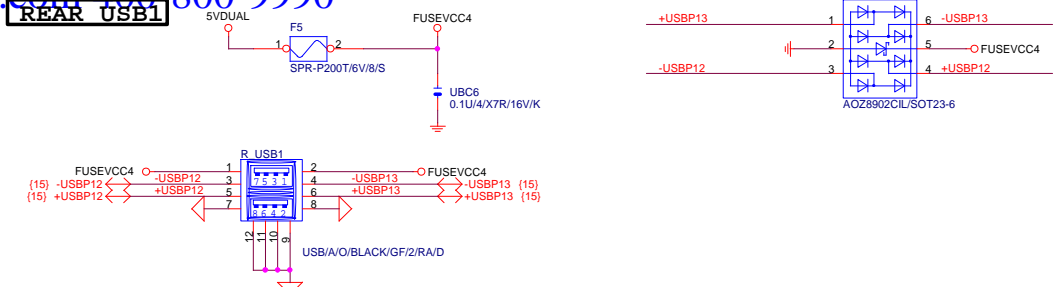
FRONT SIDE USB2



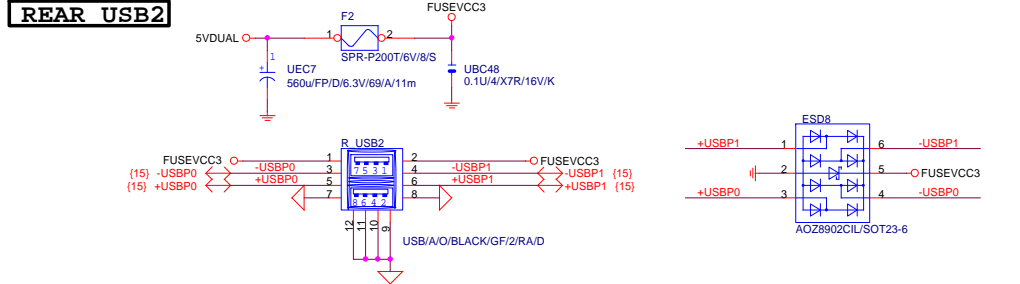
FRONT SIDE USB3



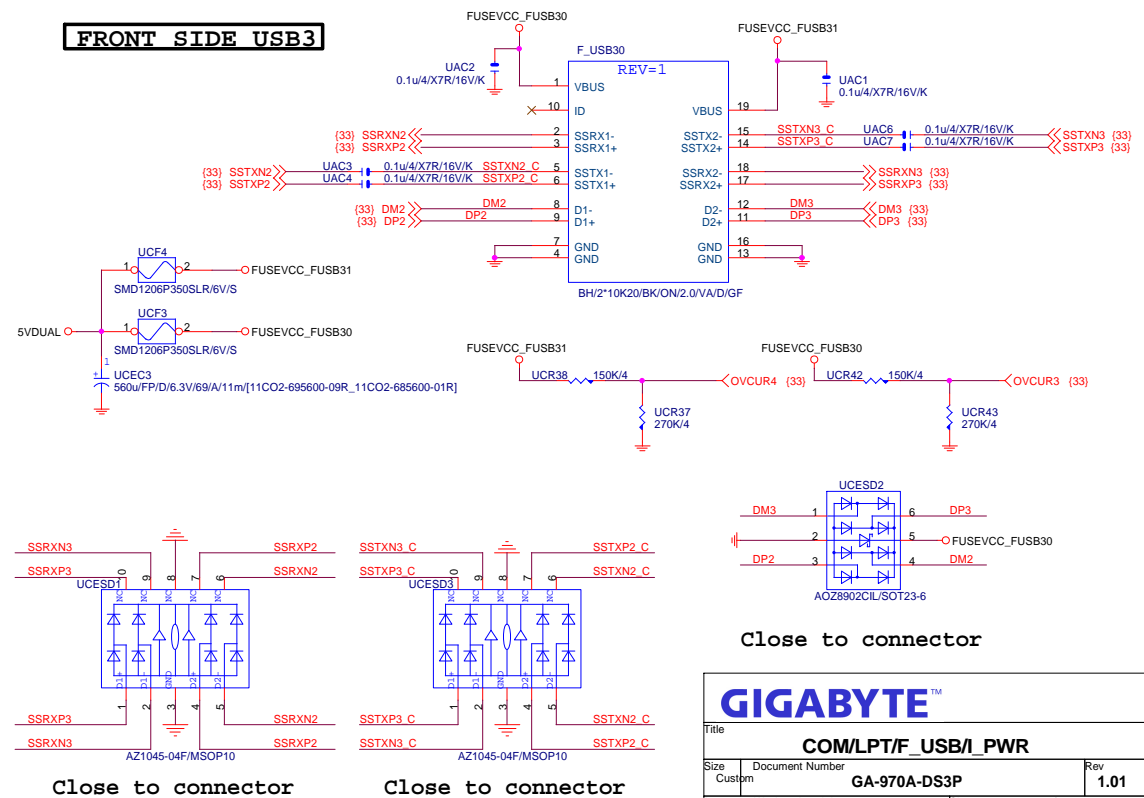
REAR USB1



REAR USB2



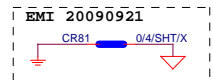
FRONT SIDE USB3



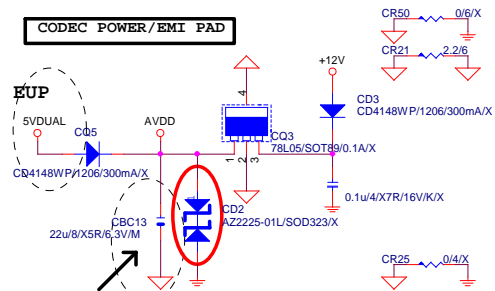
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COM/LPT/F_USB/I_PWR

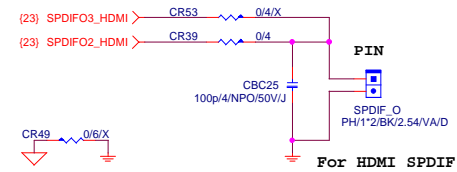
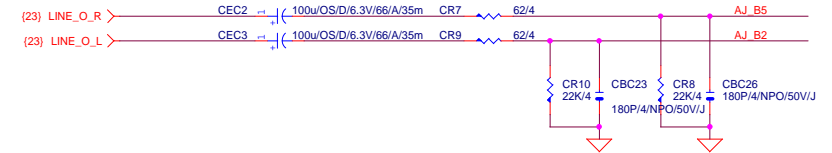
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CODEC POWER/EMI PAD



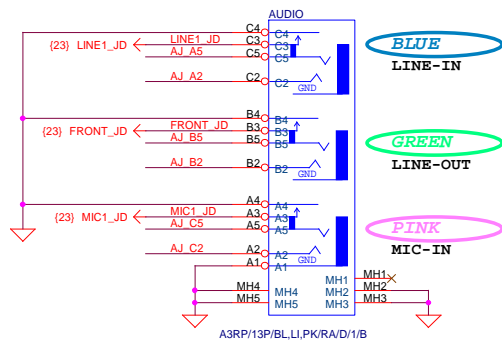
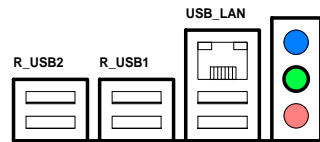
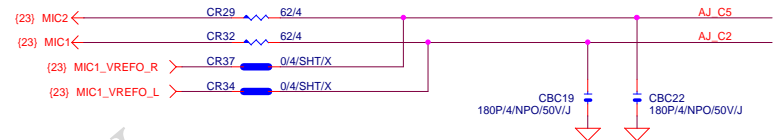
SPDIF

LINE OUT
FRONT OUT

LINE-IN



MIC

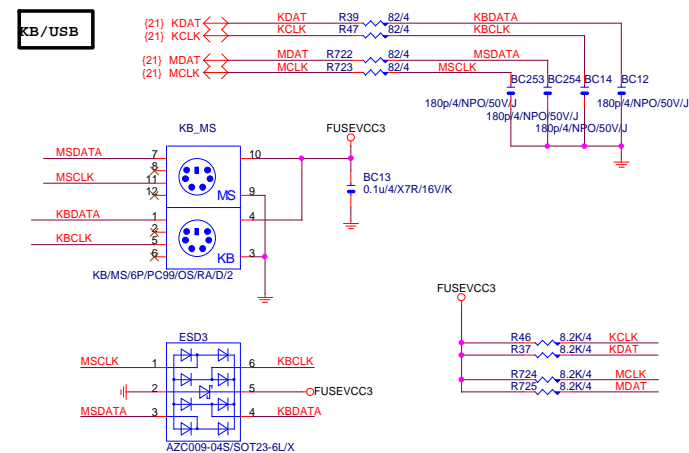
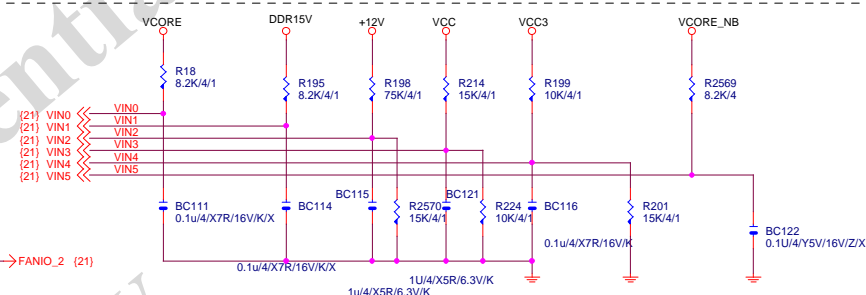
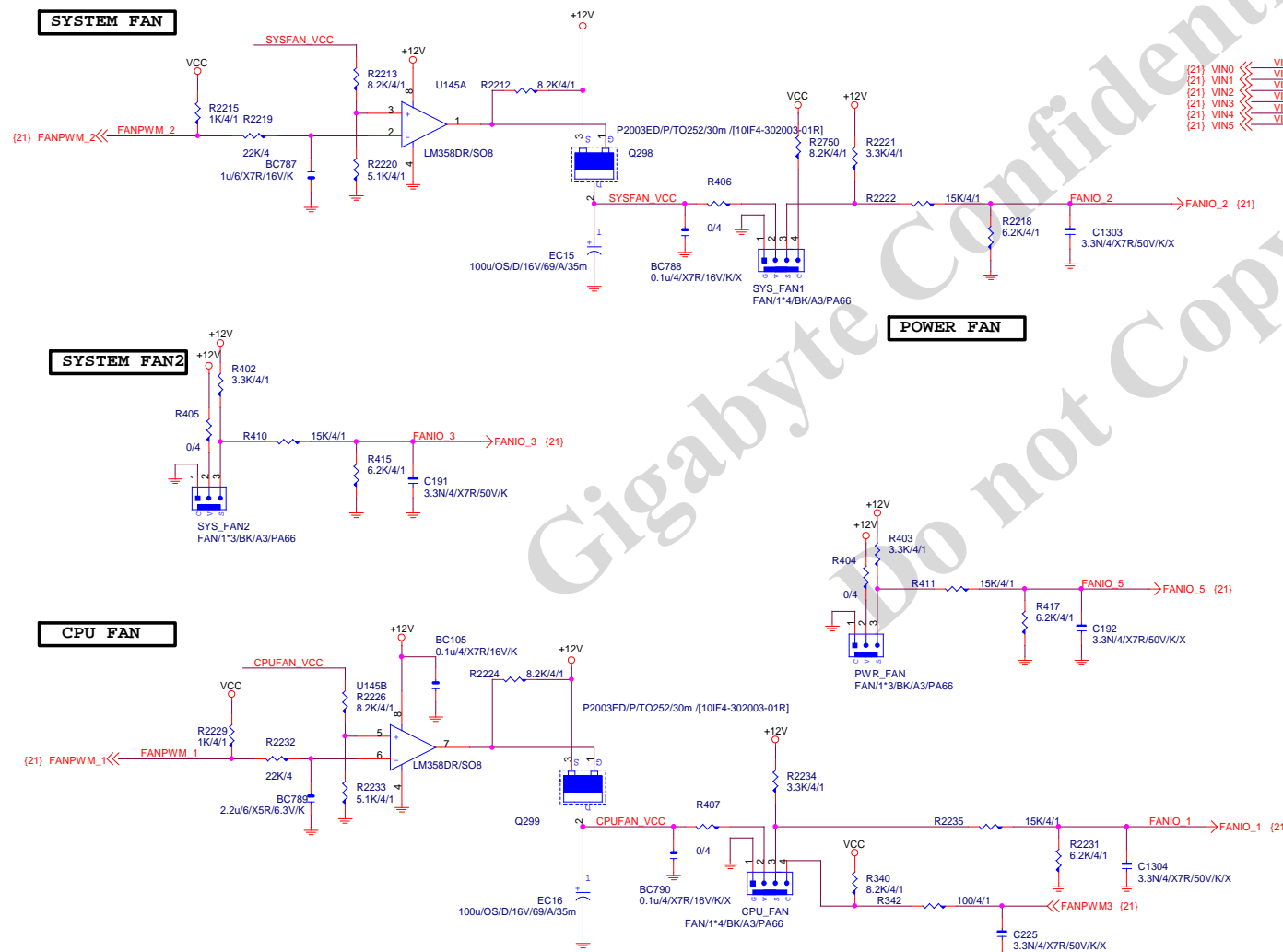
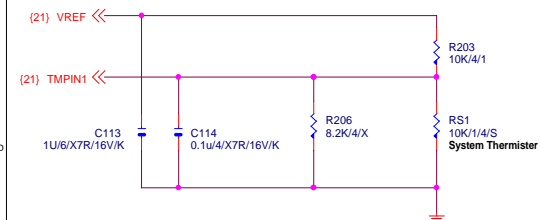


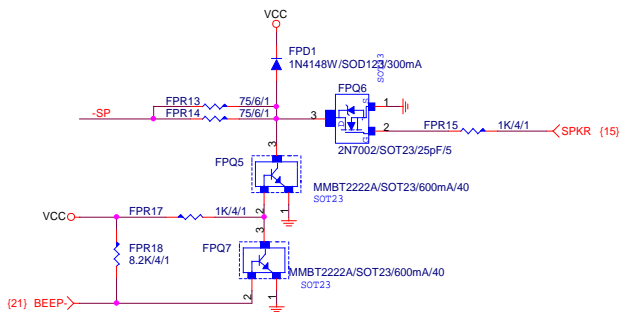
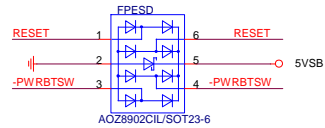
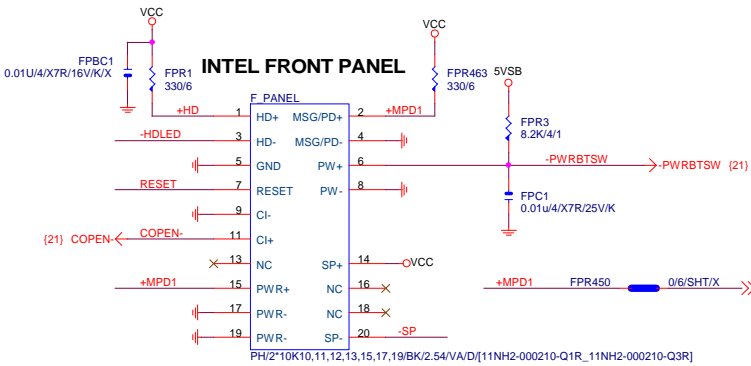
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Title
AUDIO JACKSize
Custom Document Number
GA-970A-DS3PRev
1.01

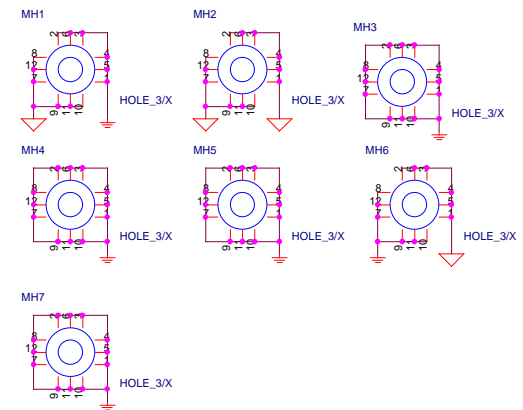
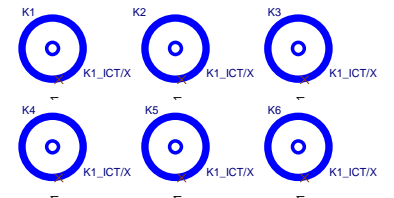
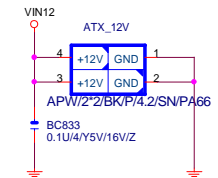
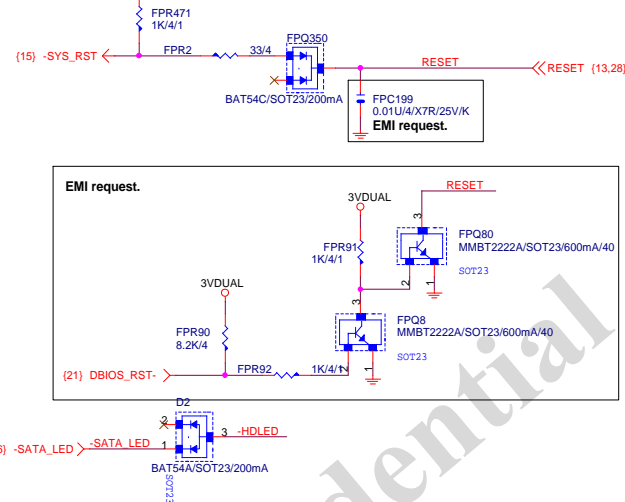
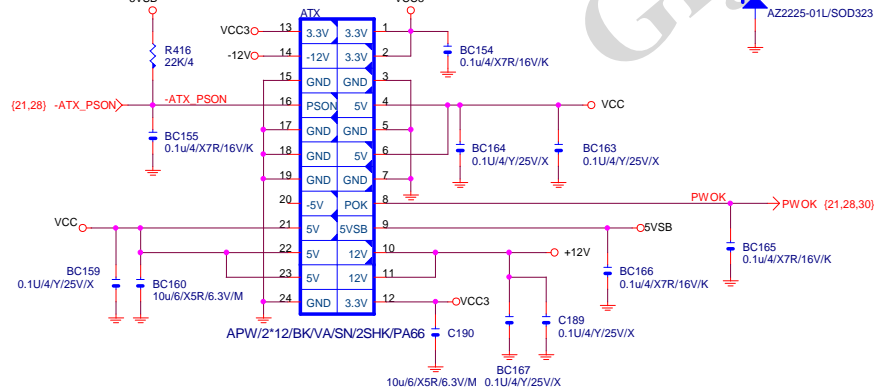
Date: Wednesday, July 02, 2014 Sheet 24 of 33

Hardware Monitor circuits





ATX POWER CONNECTOR



www.xinxunwei.com 400-800-9990

RT8868

RT9612B

ISL6330G

PROCHOT

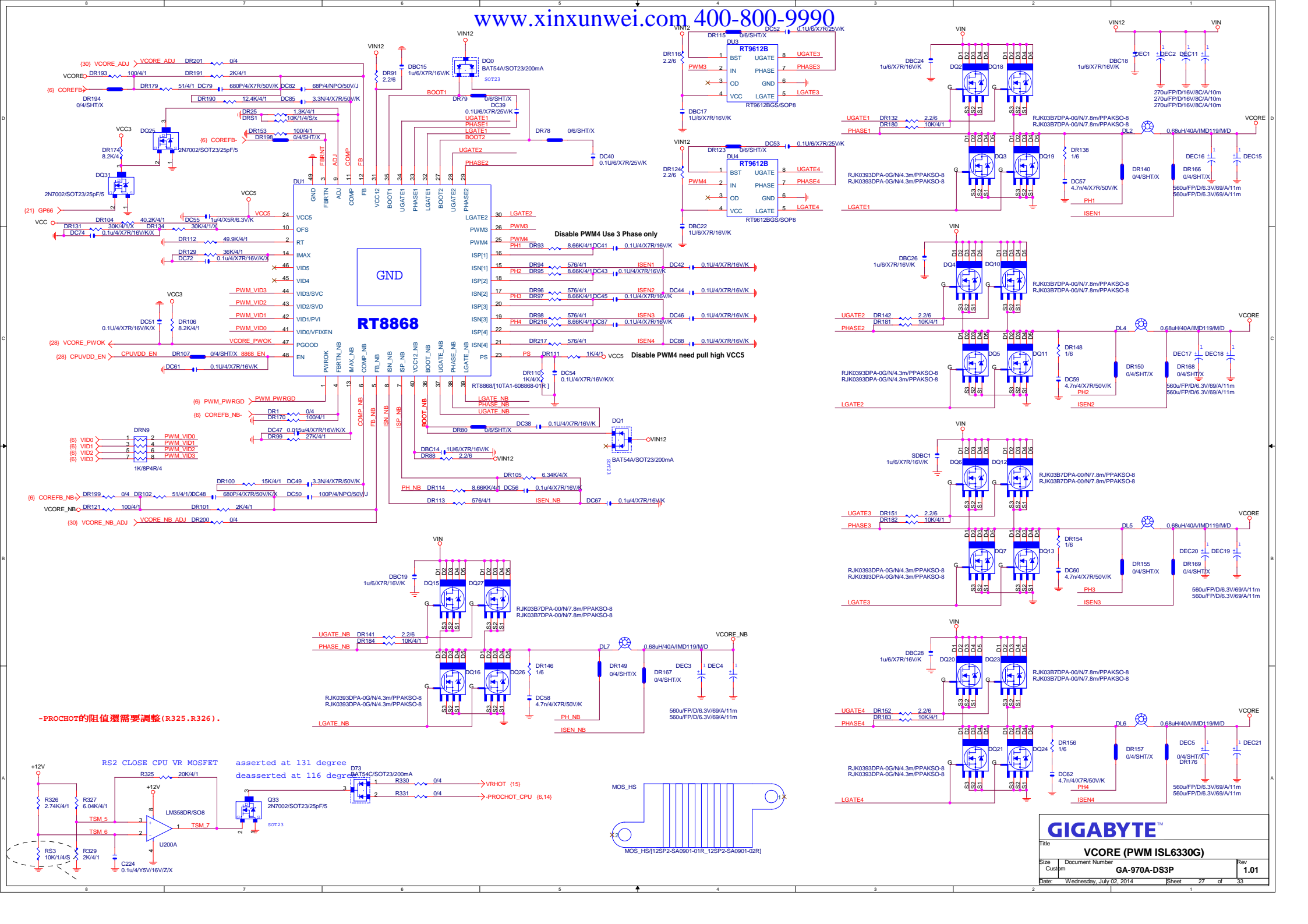
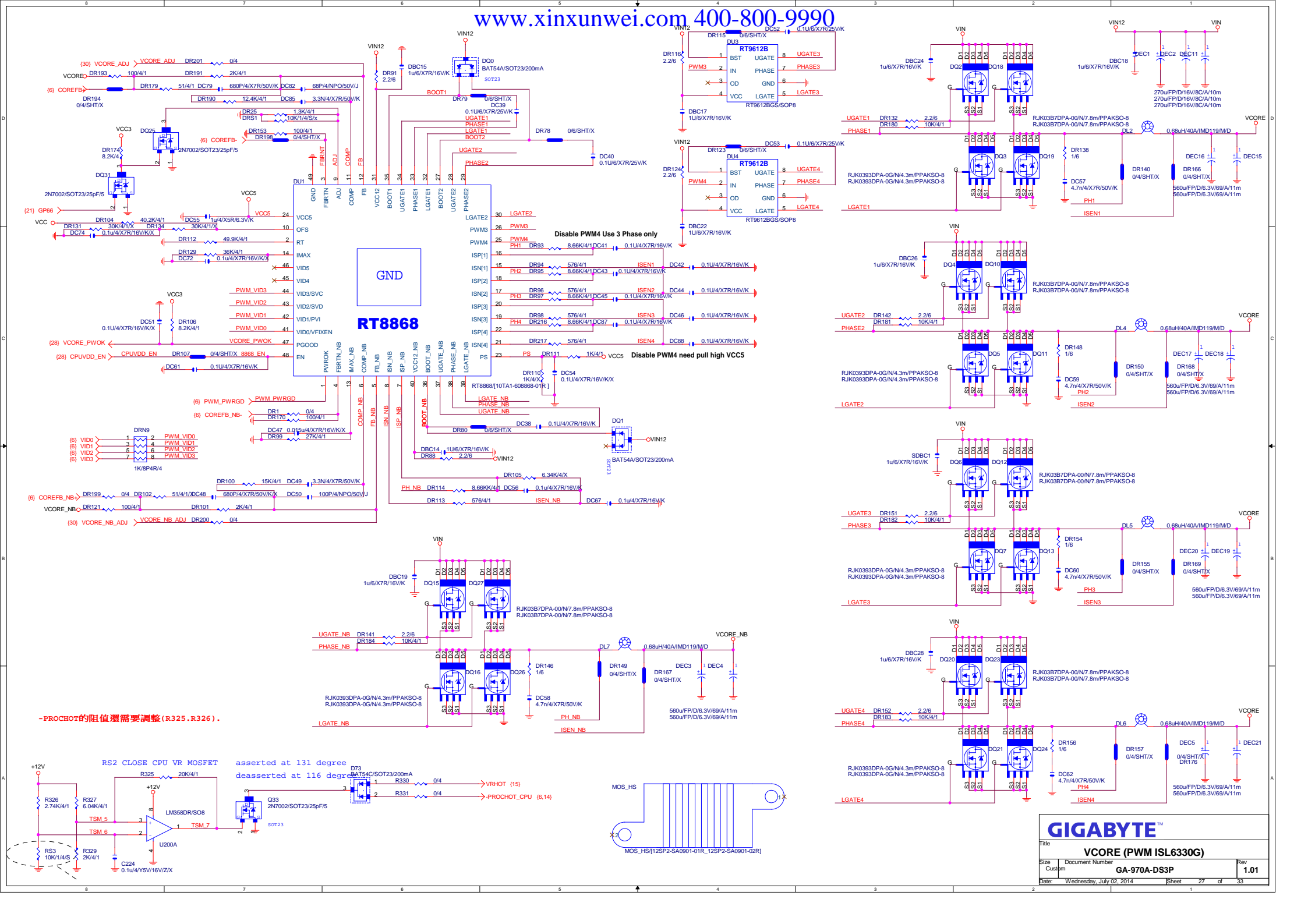
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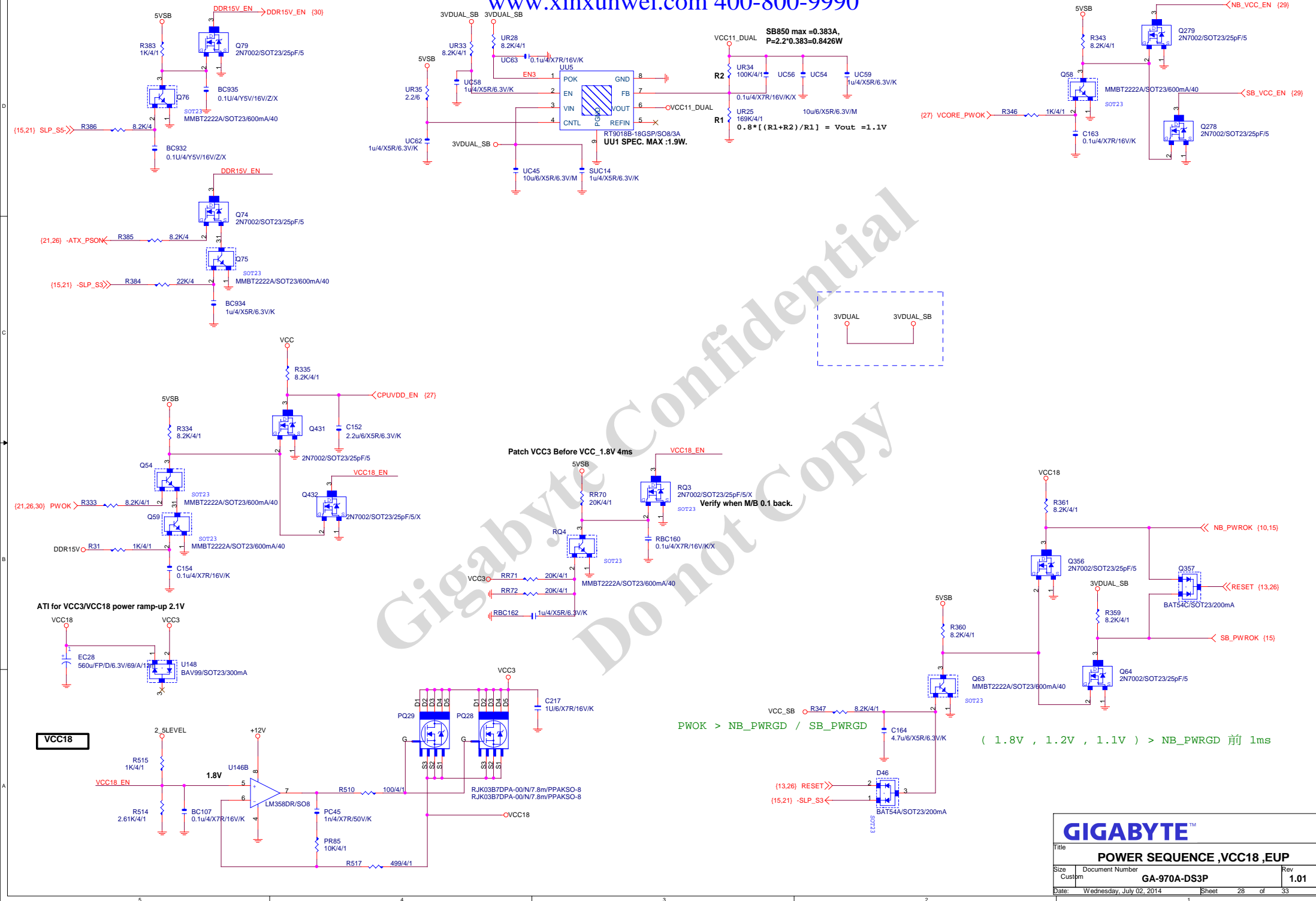
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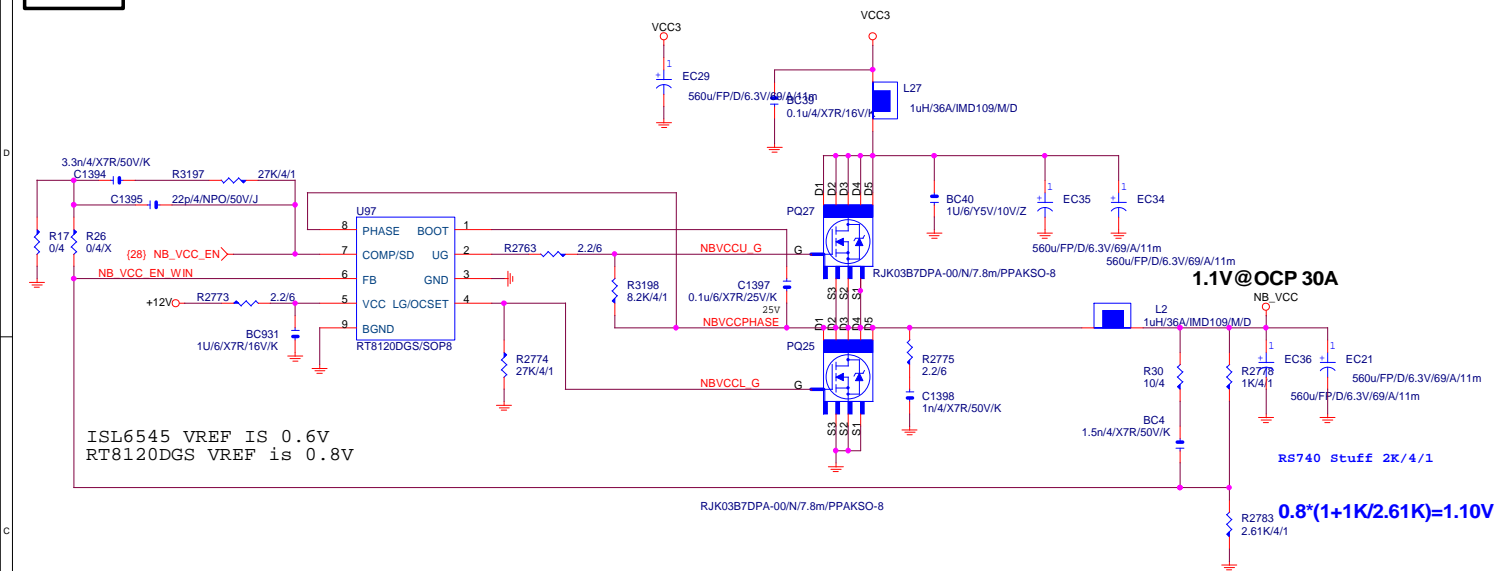
VCORE (PWM ISL6330G)

Rev 1.01

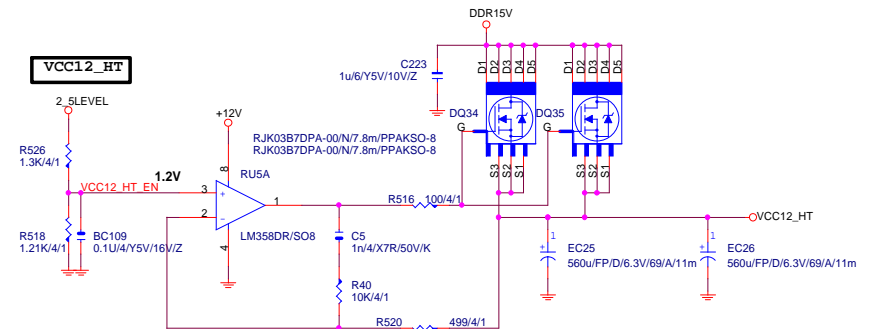




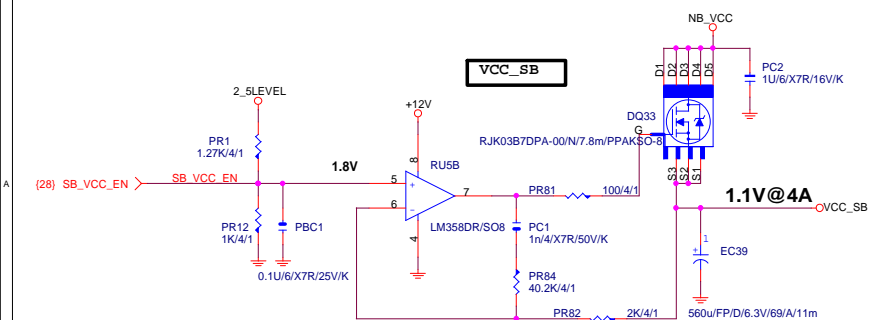
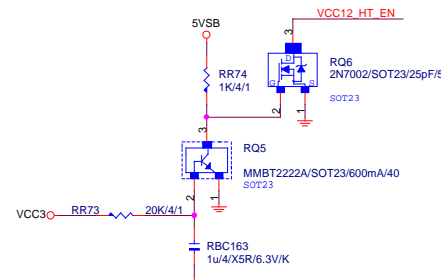
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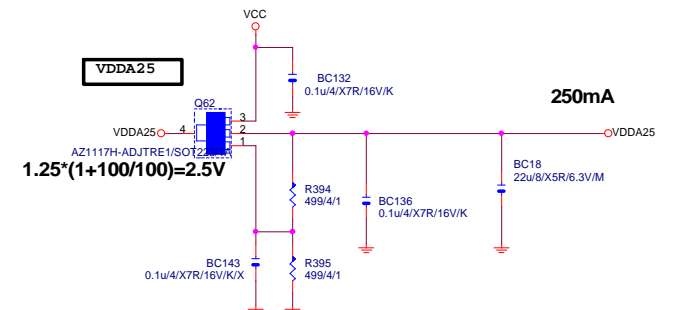
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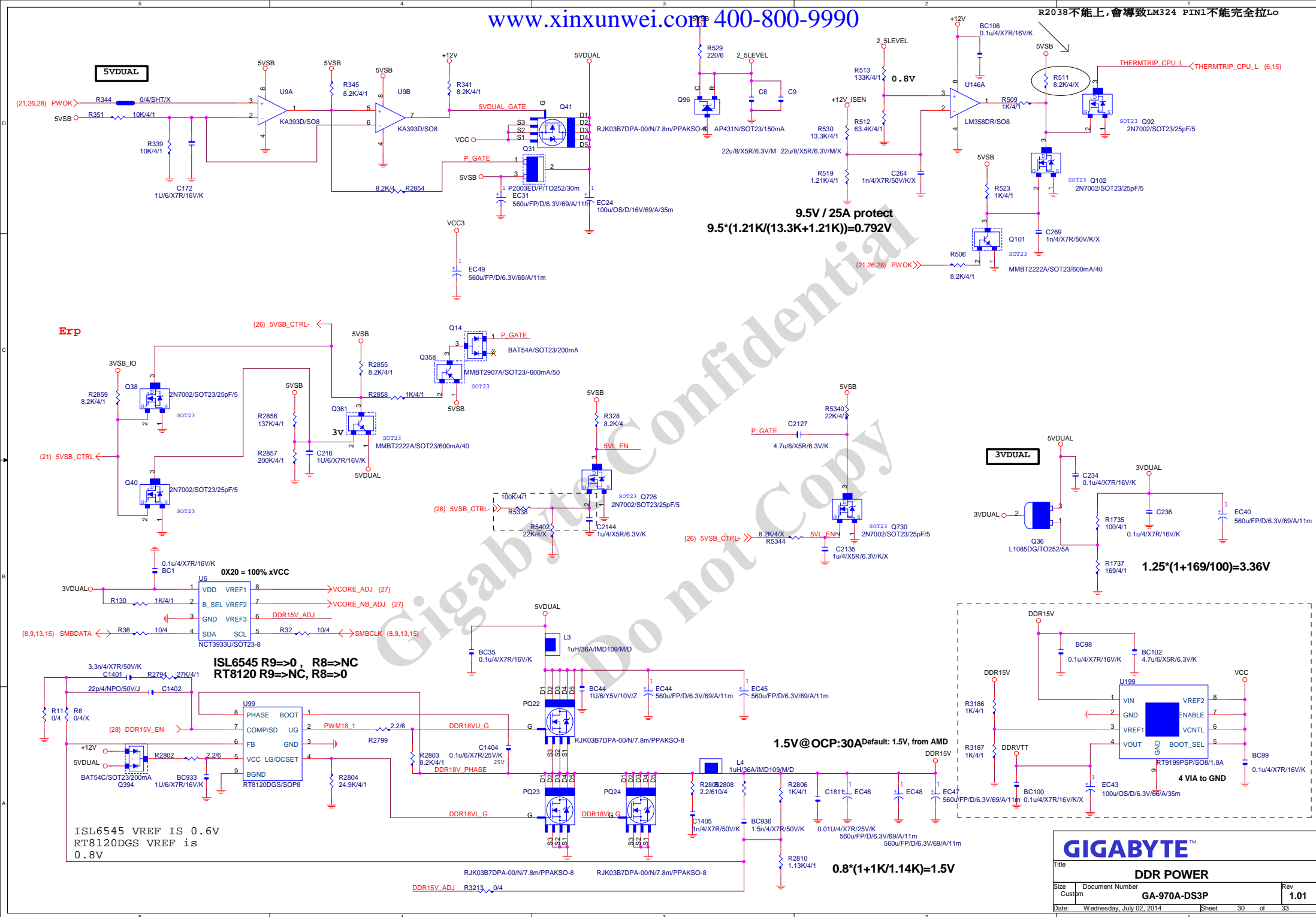
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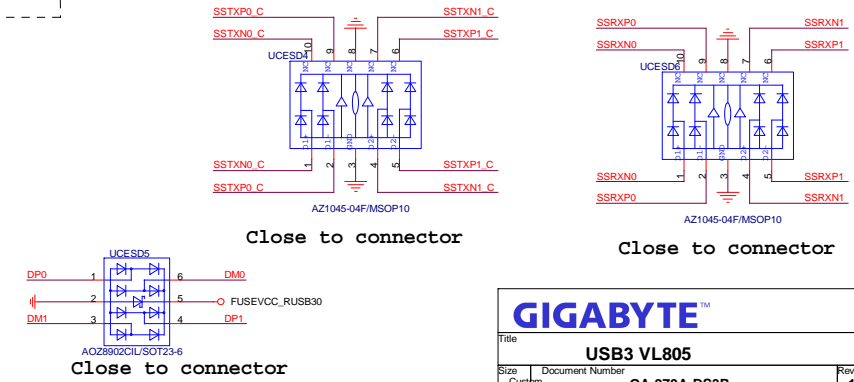
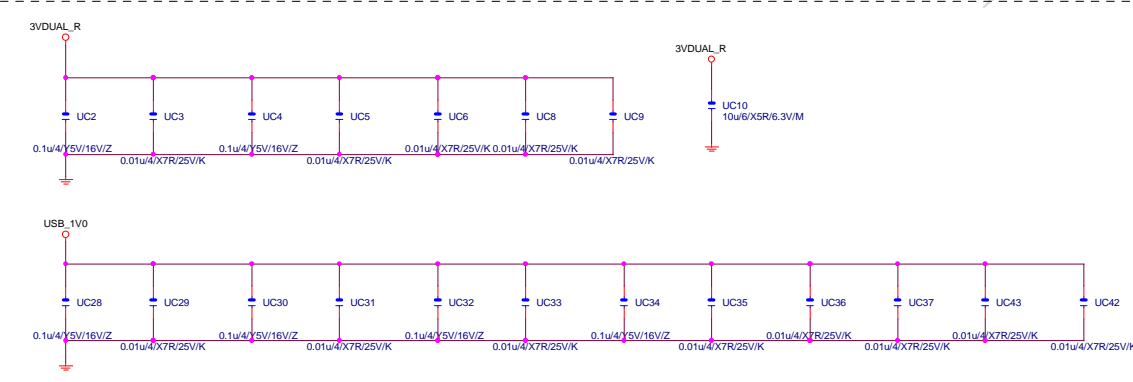
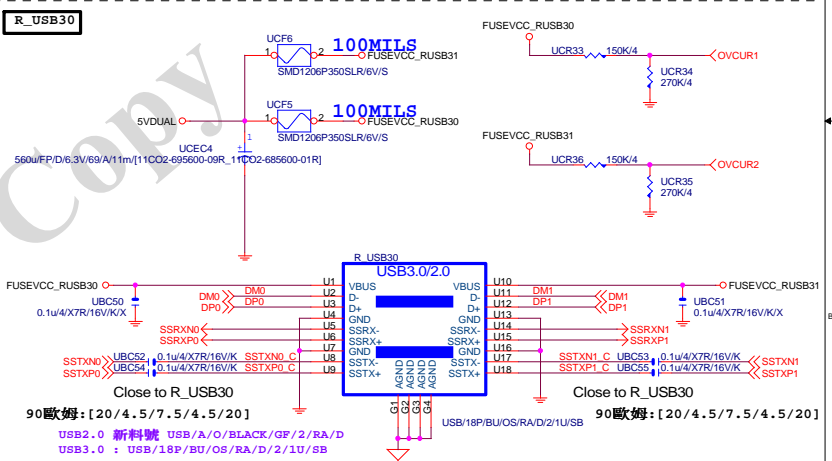
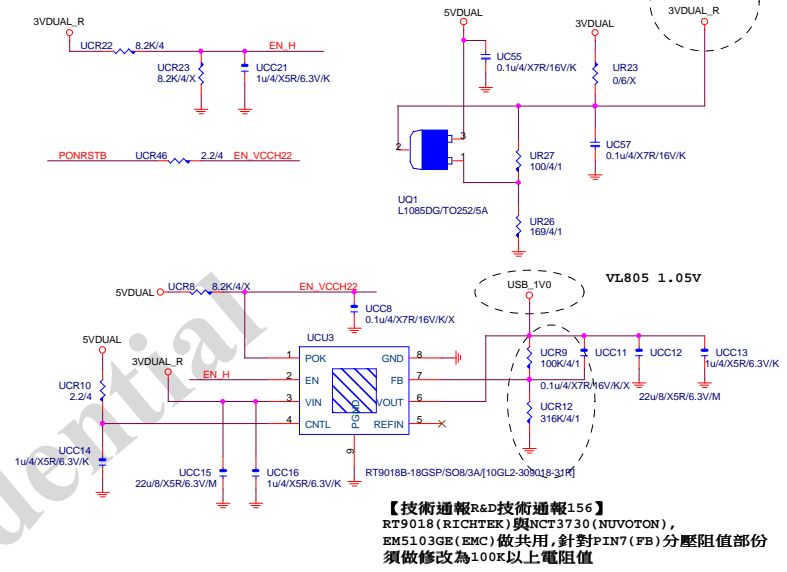
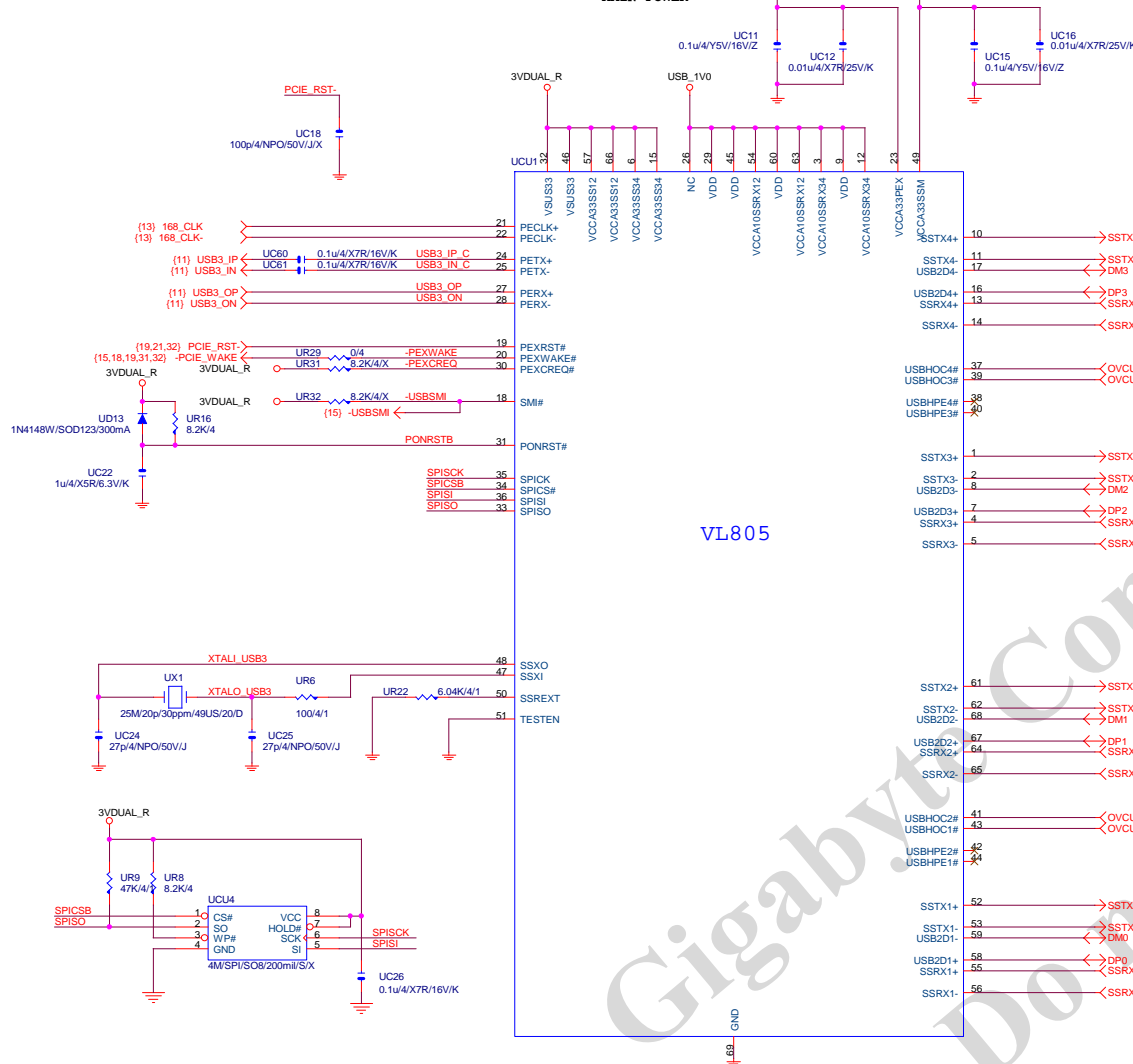
Patch AMD Validation
VDDA25 & VCC12_HT
power sequence

VDDA25



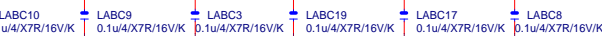
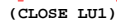
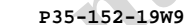
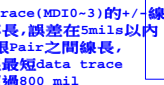
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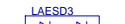




要用1% 的電阻,trace不能太長,建議在200 mil以內



RTL8102E:LC5/LC6-->0



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1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```

